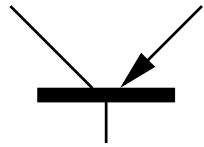
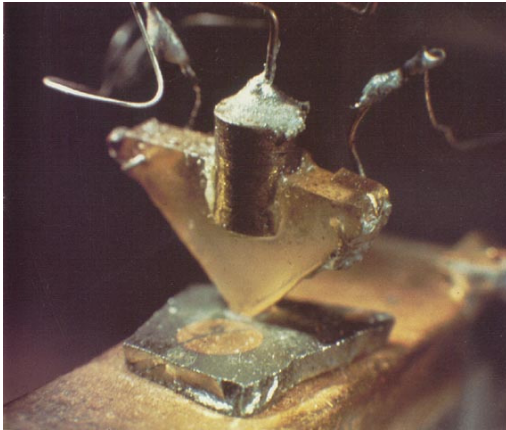
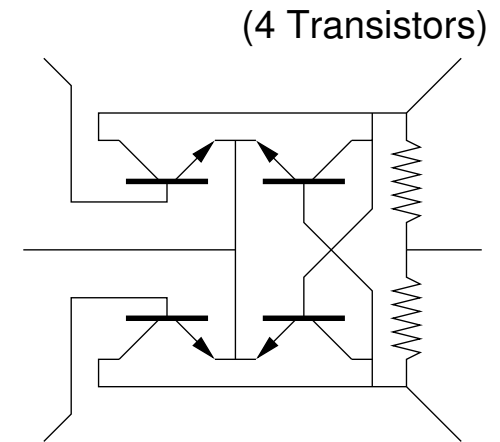
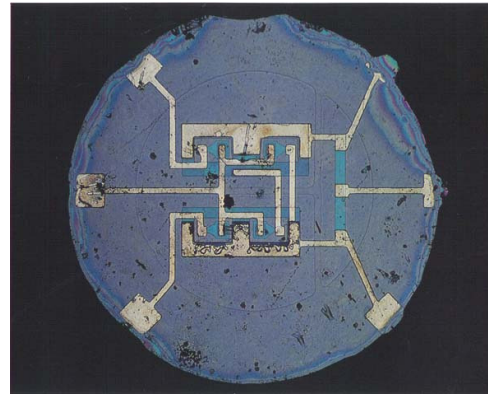


1947 Point Contact transistor

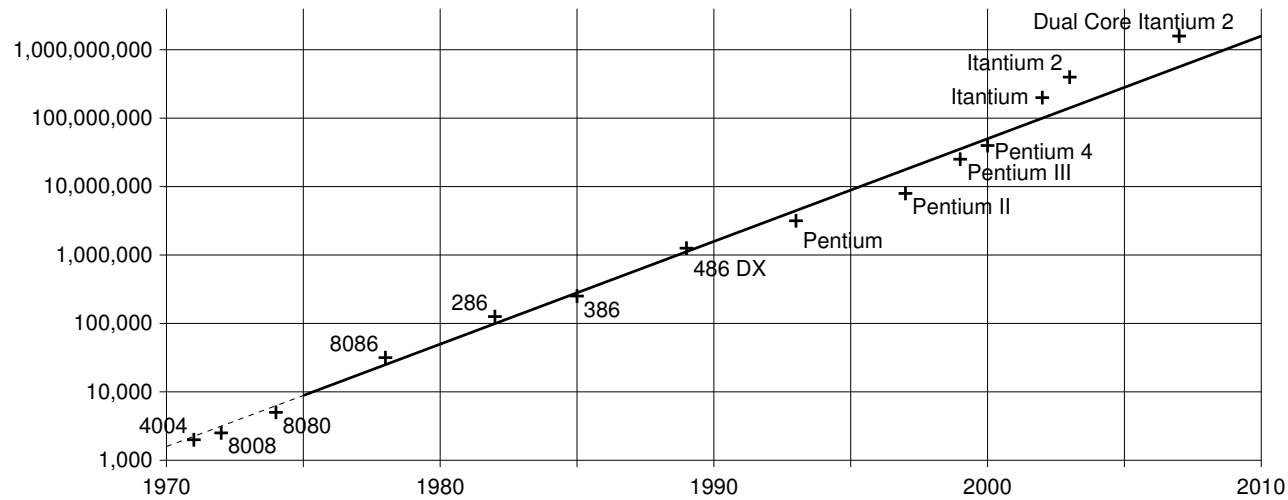


1961 Fairchild Bipolar RTL RS Flip-Flop



1965 Moore's Law (Mk I) Number of transistor has doubled every year and will continue to do so until 1975

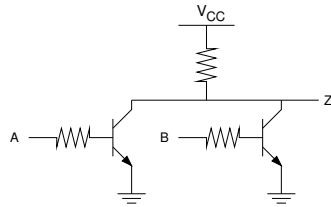
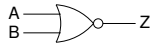
1975 Moore's Law (Mk II) Number of transistors will double every two years



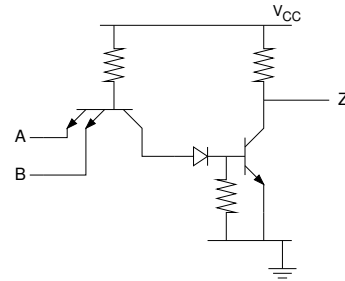
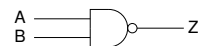
Self-fulfilling Prophecy

1000

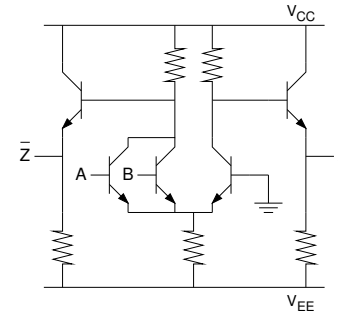
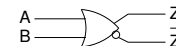
RTL NOR Gate



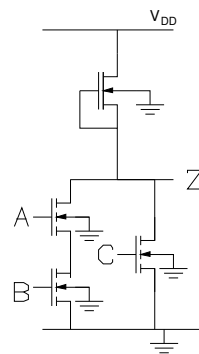
TTL NAND Gate



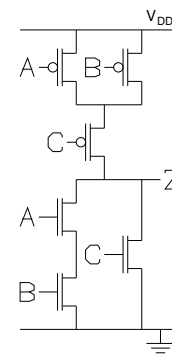
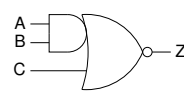
ECL OR/NOR Gate



NMOS Compound Gate



CMOS Compound Gate



- Bipolar Transistors with Resistors - MSI/LSI

RTL - NOR

TTL - NAND

ECS - OR/NOR

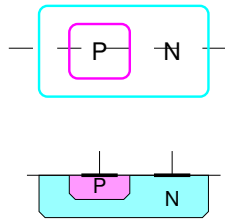
- MOS Transistors (no resistors) - VLSI

NMOS

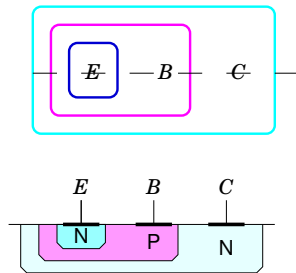
CMOS - No static power!

Both allow construction of NOR, NAND & Compound gate (always inverting)

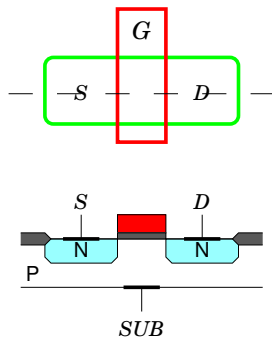
Diode



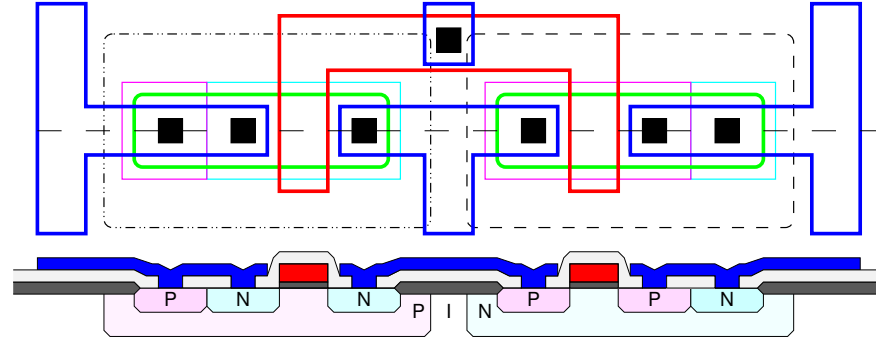
NPN Transistor



NMOS Enhancement transistor
NMOS Process



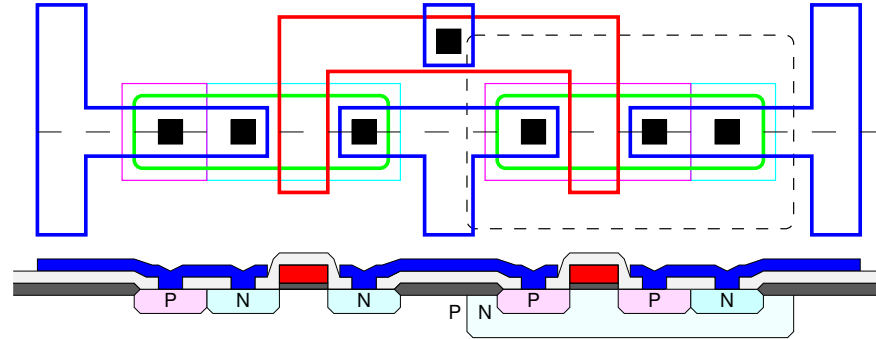
CMOS Inverter



Twin Tub CMOS Process

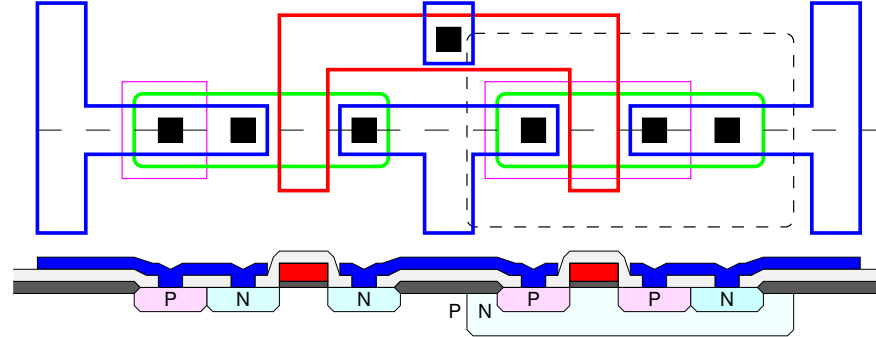
CMOS Inverter

N-Well CMOS Process (with explicit N+ implant mask)



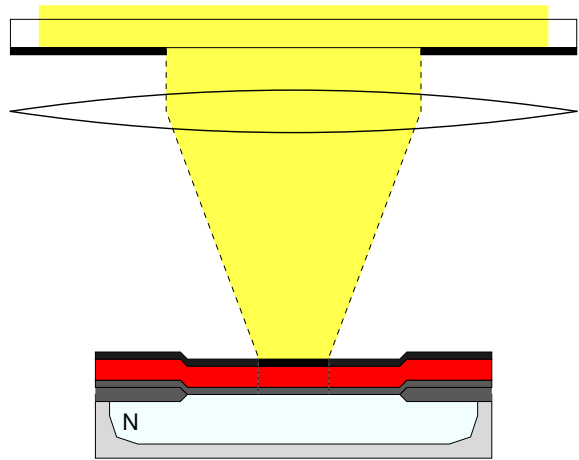
CMOS Inverter

N-Well CMOS Process (without explicit N+ implant mask)

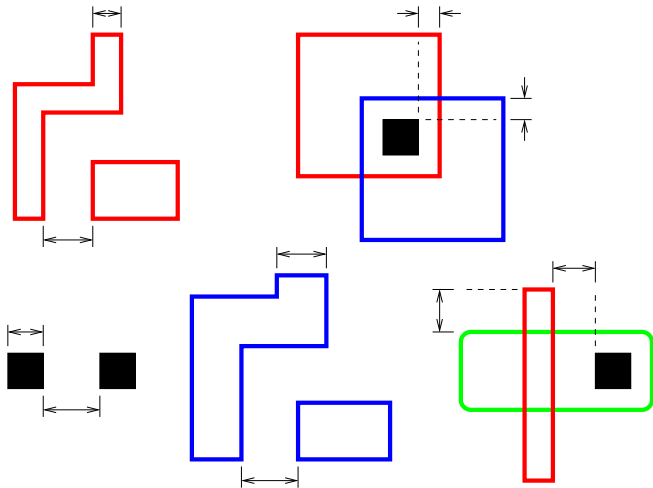


Features may be determined by a number of masks
 e.g. NMOS source drain: ActiveArea AND NOT(NWell OR Poly OR PImplant)

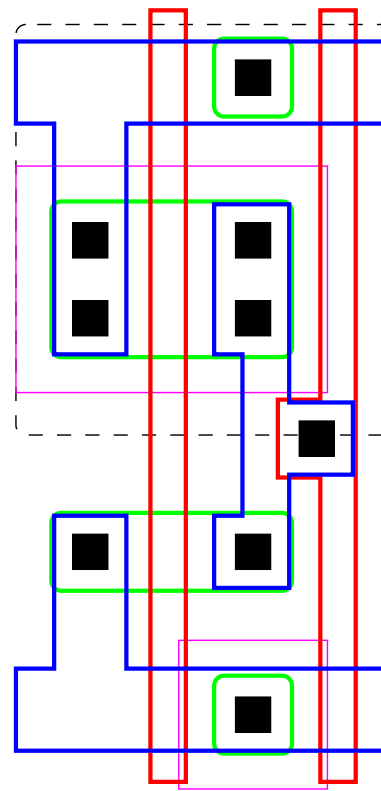
Processing



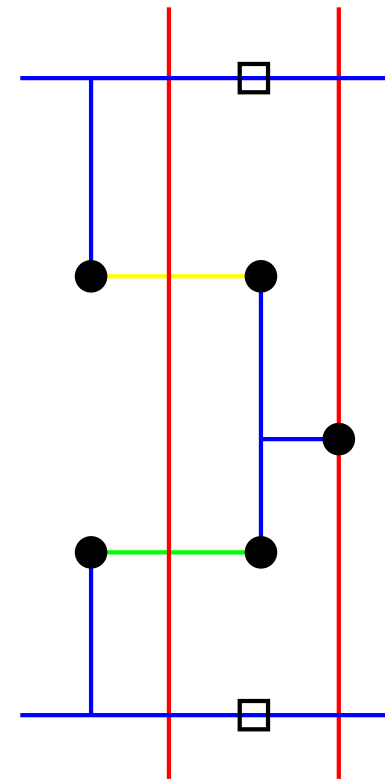
Design Rules – width, separation, overlap



Optimised Mask Layout

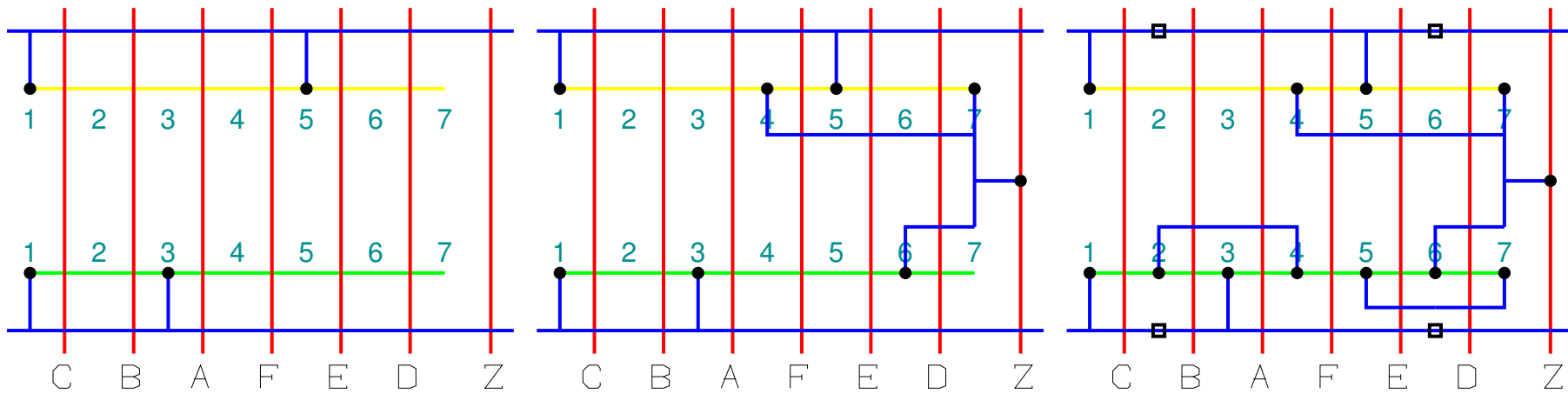
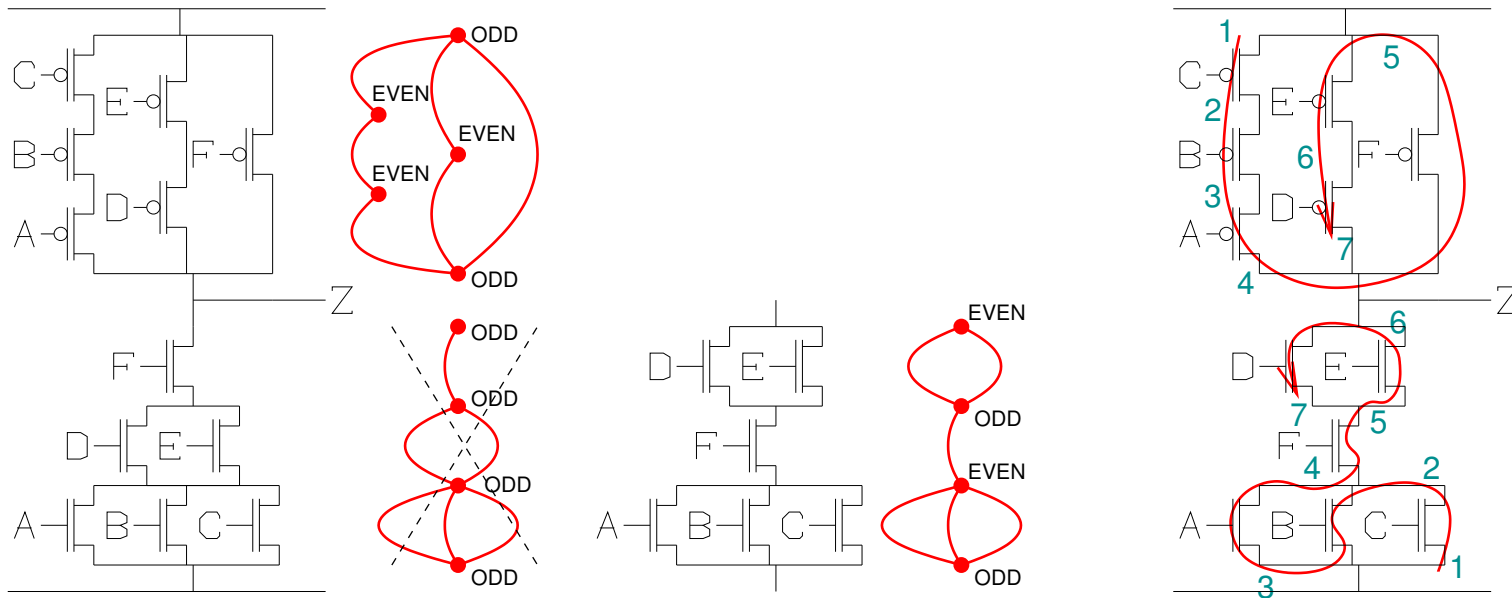


Equivalent Stick Diagram



- Metal
- Polysilicon
- N+
- P+
- Contact
- Tap
- Combined contact & tap

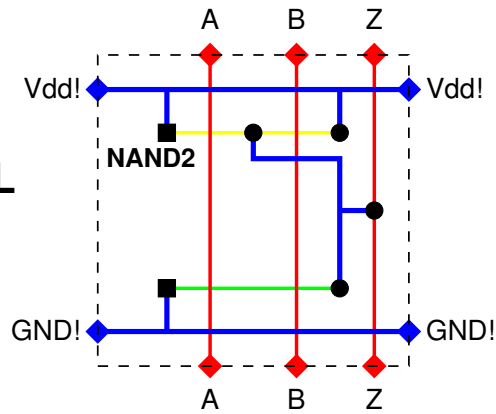
Investigation of Euler paths leads to more efficient layout*



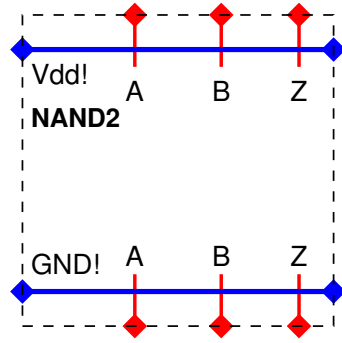
*not all gates will support a common Euler path for both PMOS and NMOS

1 METAL LAYER

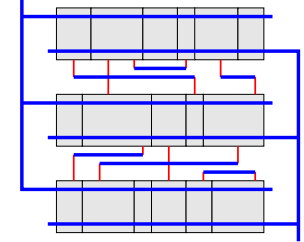
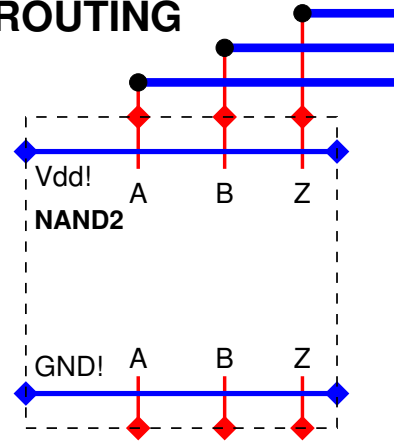
LAYOUT



ABSTRACT

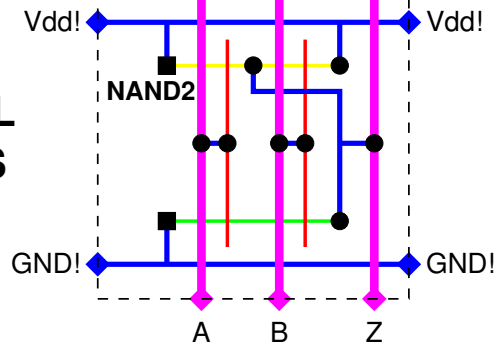


ROUTING

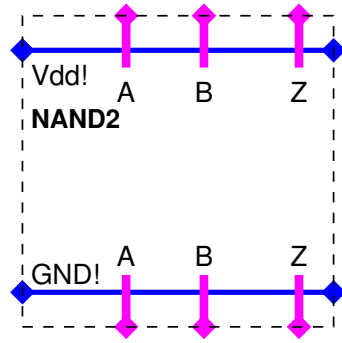


2 METAL LAYERS

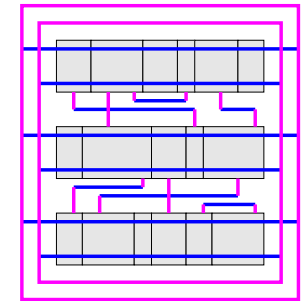
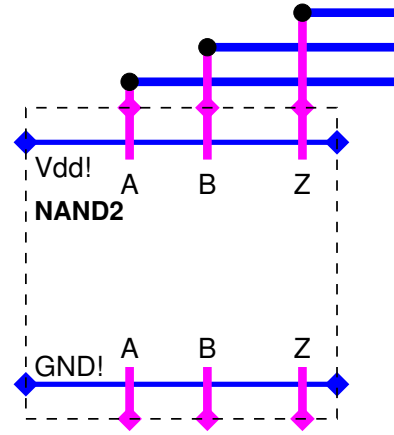
LAYOUT



ABSTRACT

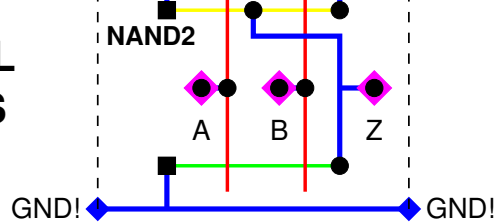


ROUTING

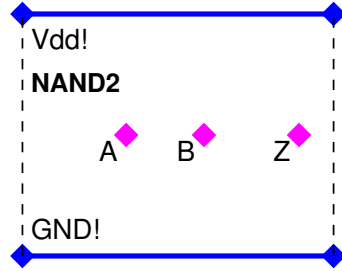


3 METAL LAYERS

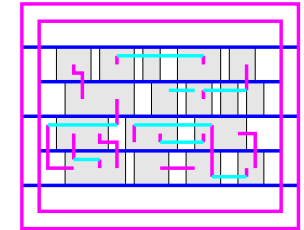
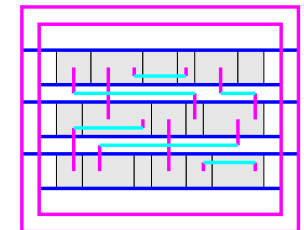
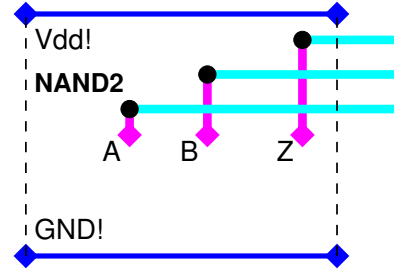
LAYOUT



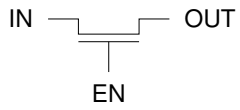
ABSTRACT



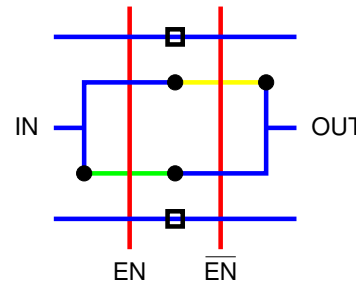
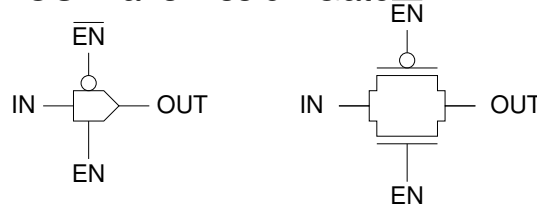
ROUTING



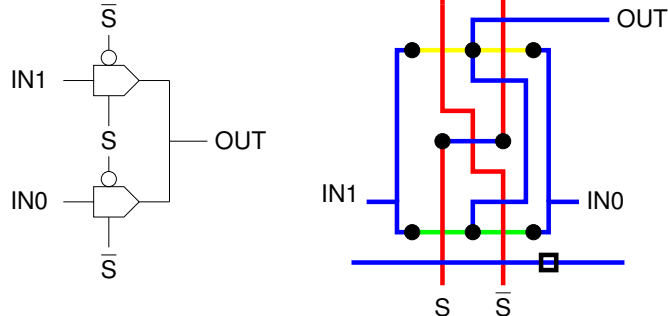
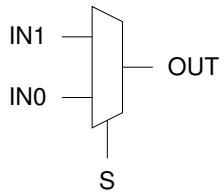
Pass Transistor



CMOS Transmission Gate



Transmission Gate Multiplexor

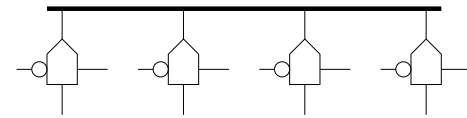


*note distinctive polysilicon crossover

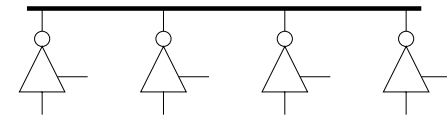
Tri-state gates are used for Multiplexing

Distributed Multiplexing

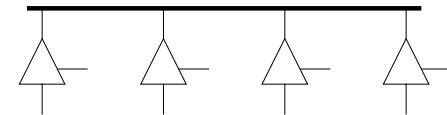
using transmission gates



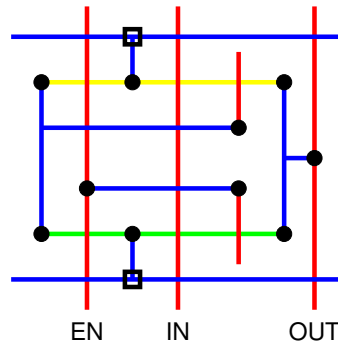
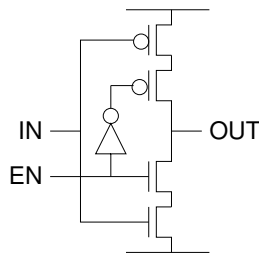
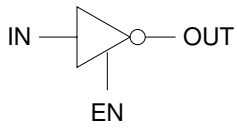
using tri-state inverters



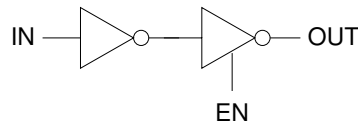
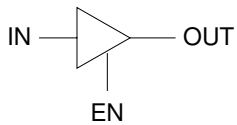
using tri-state buffers



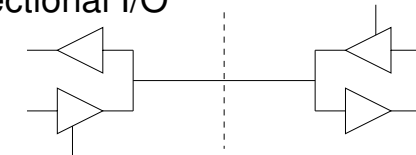
Tri-state Inverter



Tri-state Buffer

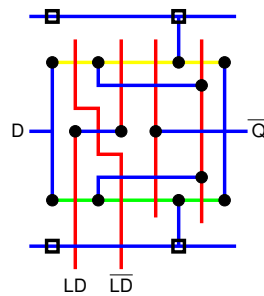
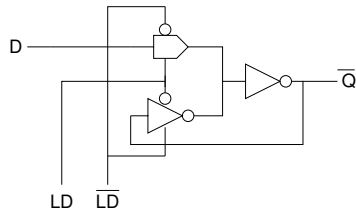
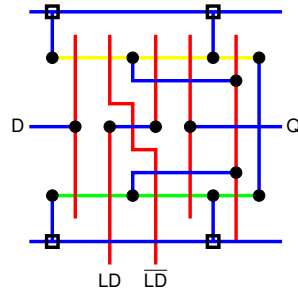
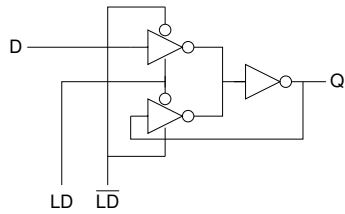


Bi-directional I/O

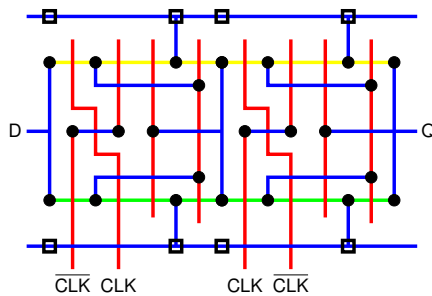
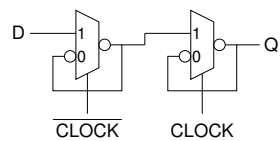
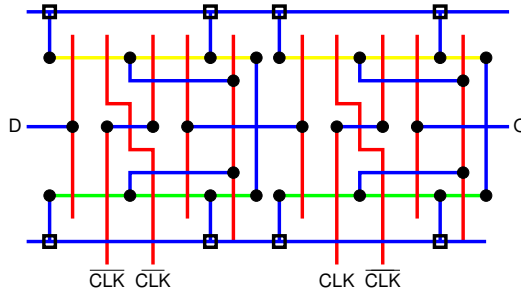
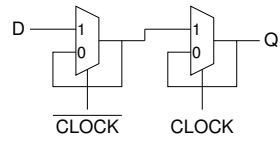


*this is another form of multiplexing

Latch

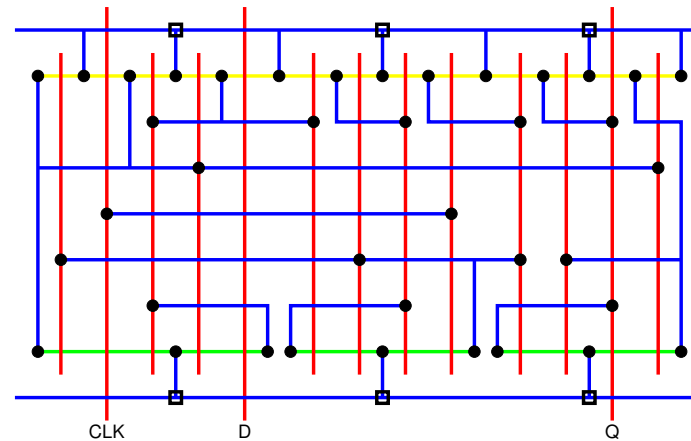
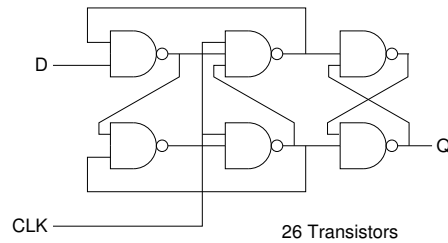


Master Slave D-Type Flip-Flop



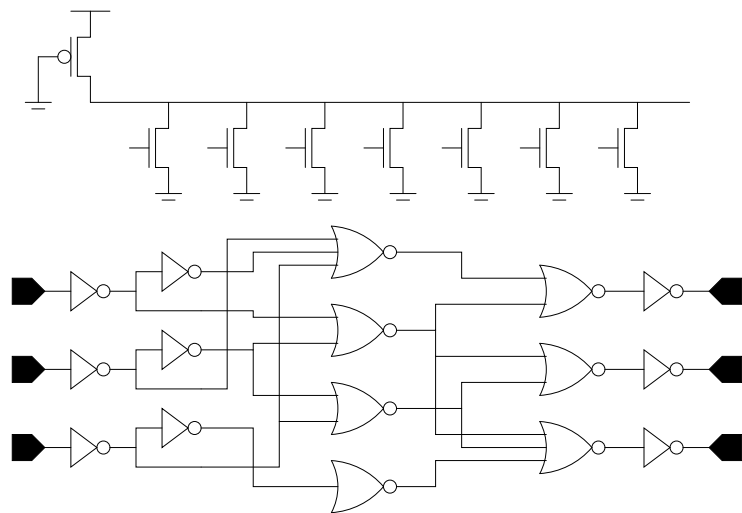
*multiplexor based latches and flip-flops include distinctive polysilicon crossover

Edge Triggered D-Type Flip-Flop



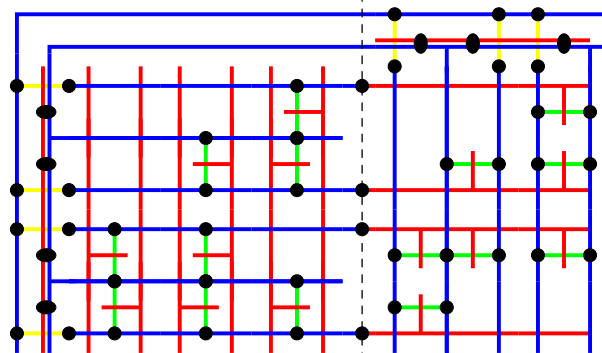
Euler path analysis is applied creatively to these multi-gate cells – gates are often linked via the common gnd/pwr node
Final layouts will be more complex where clock buffers, reset circuitry and metal 2 i/o are included

PLA and ROM



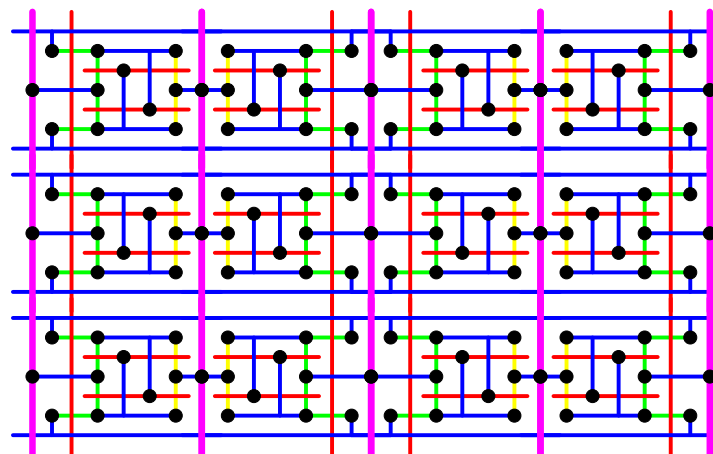
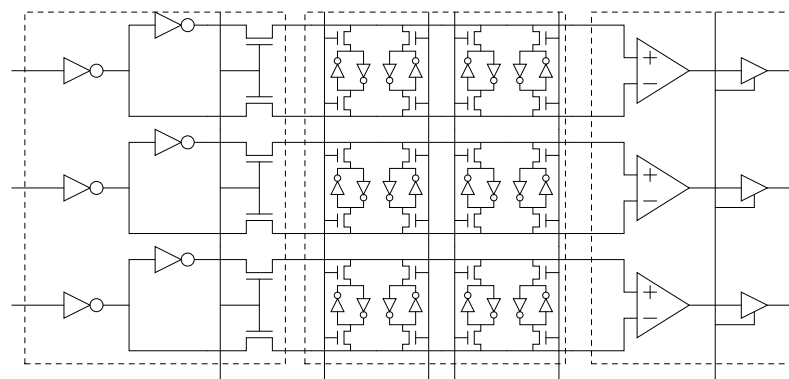
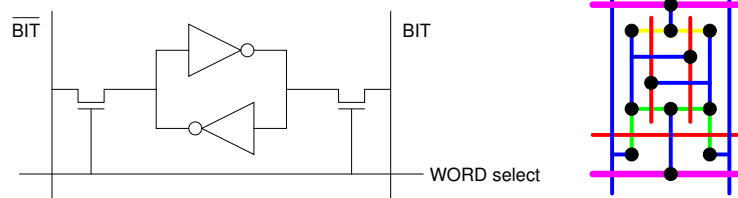
AND Plane

OR Plane



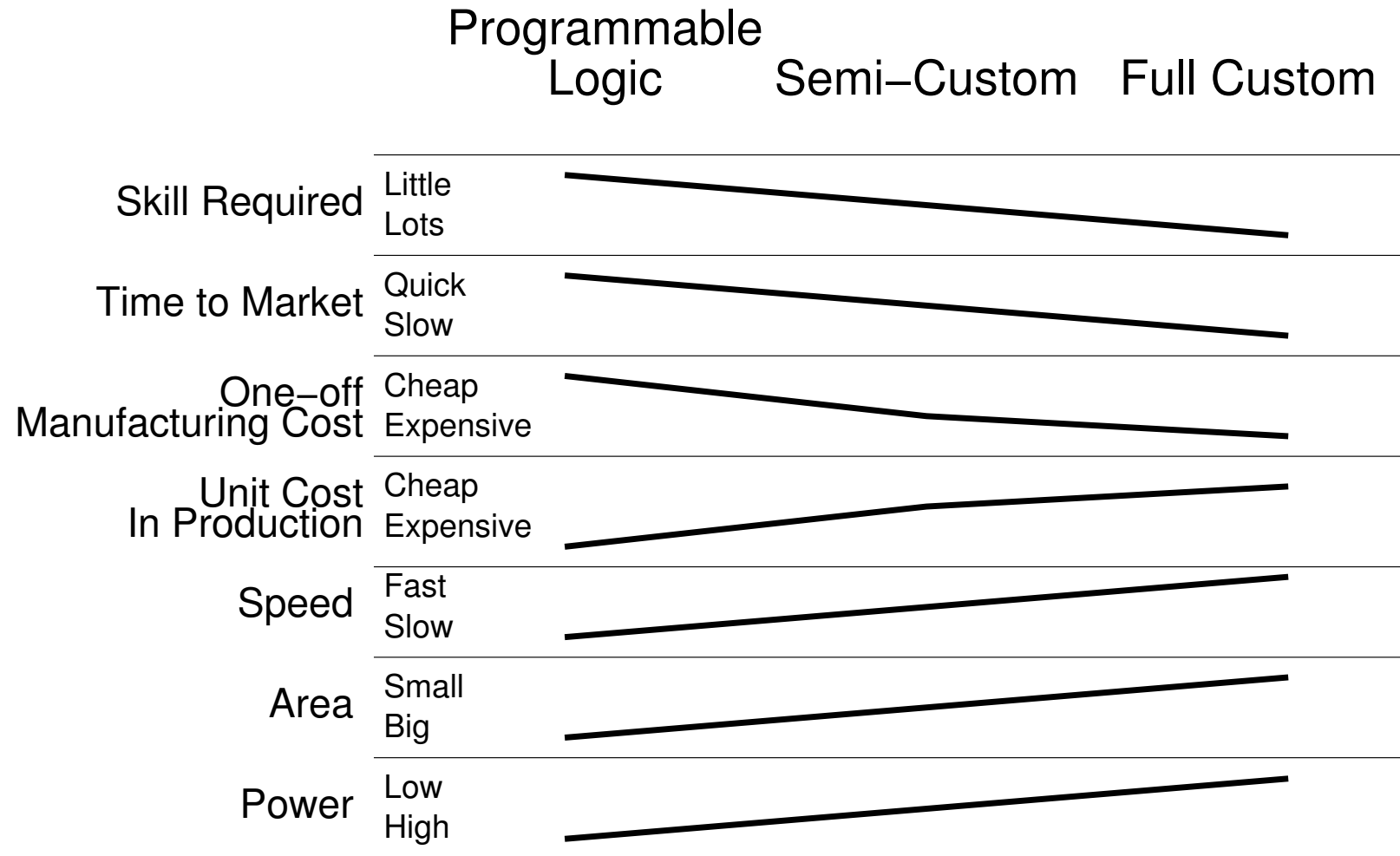
ROM is PLA with
fixed AND (decoder) plane
programmable OR (data) plane

SRAM



Cells are designed to butt together in two dimensions leading to efficient layout

PLA layout efficiency will depend on the actual function implemented (e.g. number of common product terms)



All design styles need full custom designers

A large ASIC (especially SoC) may mix Semi-Custom and Full Custom