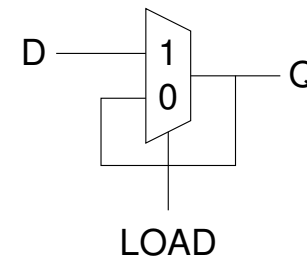
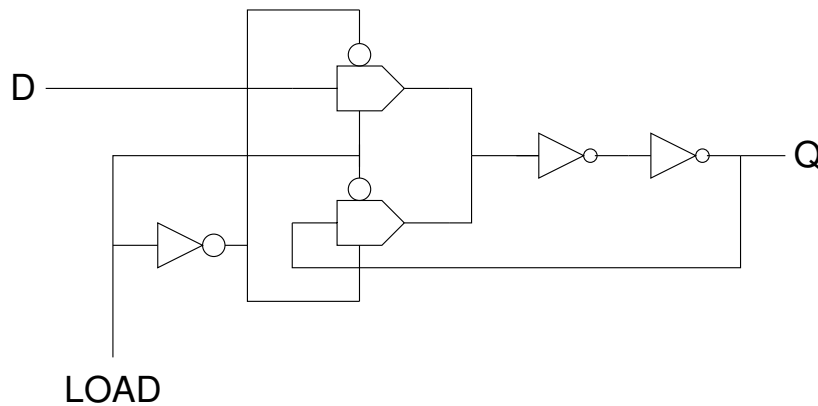


# Latches and Flip-Flops

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- CMOS transmission gate latch



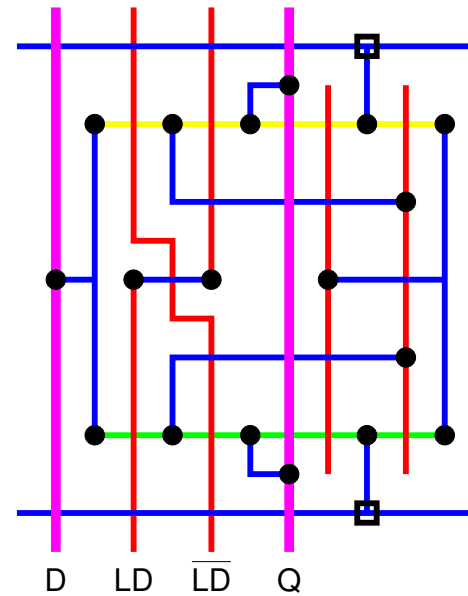
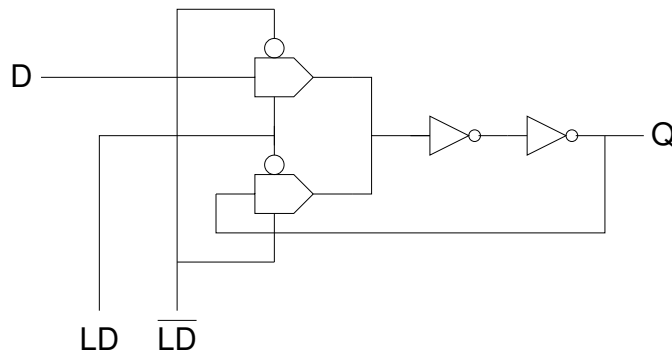
A simple transparent latch can be build around a transmission gate multiplexor

- transparent when load is high
- latched when load is low
- two inverters are required since the transmission gate cannot drive itself

# Latches and Flip-Flops

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- Transmission gate latch layout



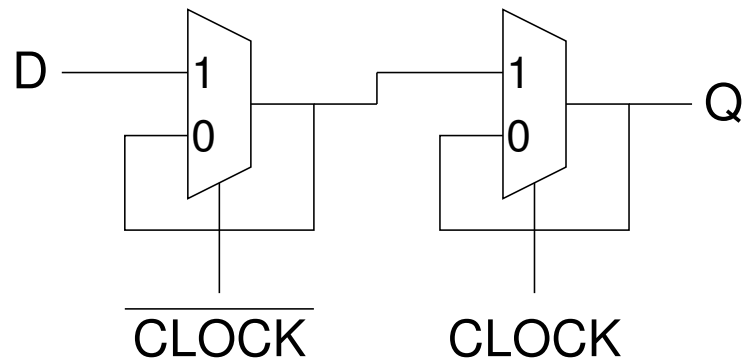
– a compact layout is possible using 2 layer metal



# Latches and Flip-Flops

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- For use in simple synchronous circuits we use a pair of latches in a master slave configuration.

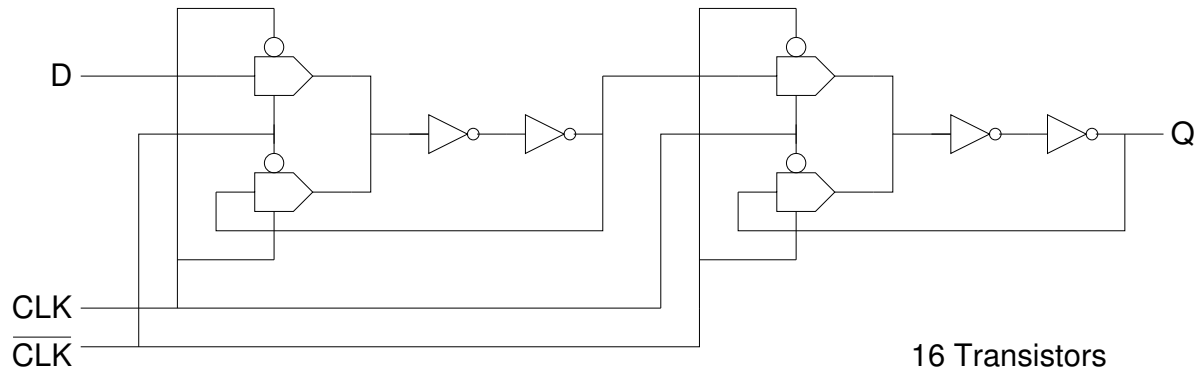


- this avoids the race condition in which a transparent latch drives a second transparent latch operating on the same clock phase.
- the circuit behaves as a rising edge triggered D type flip-flop.

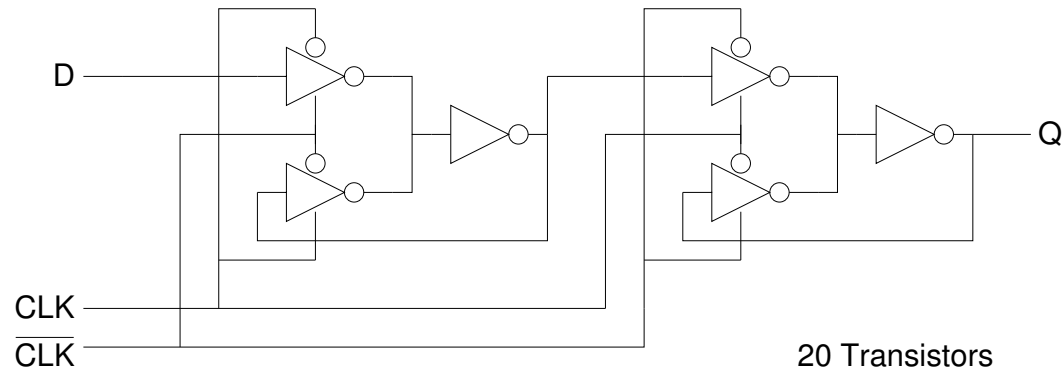
# Latches and Flip-Flops

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- Transmission gate implementation



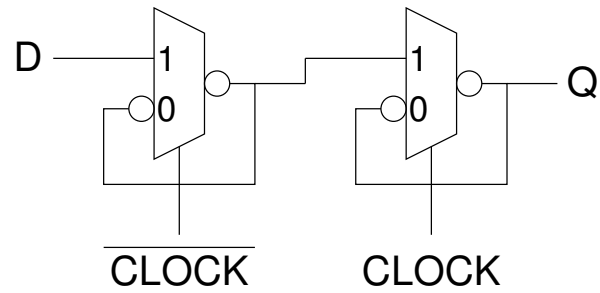
- Tristate inverter implementation



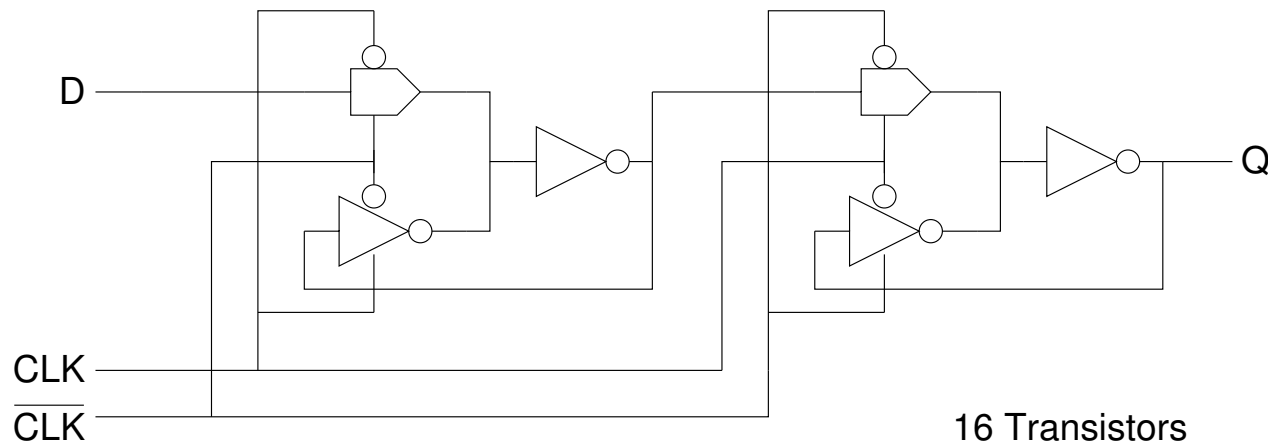
# Latches and Flip-Flops

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- Alternative configuration



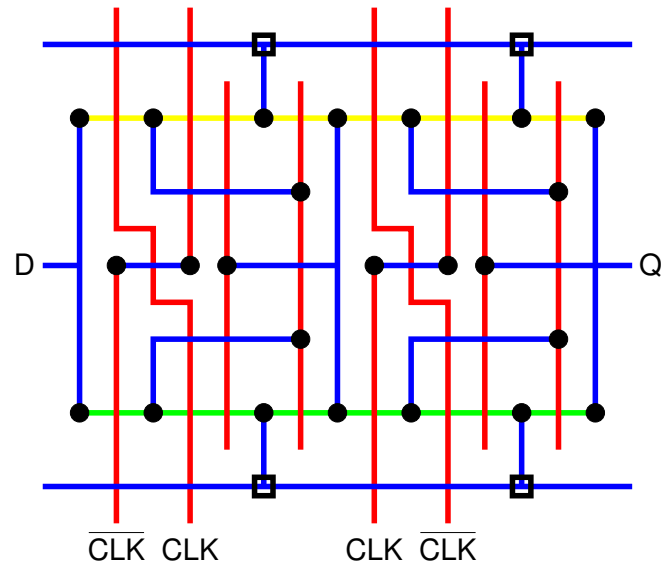
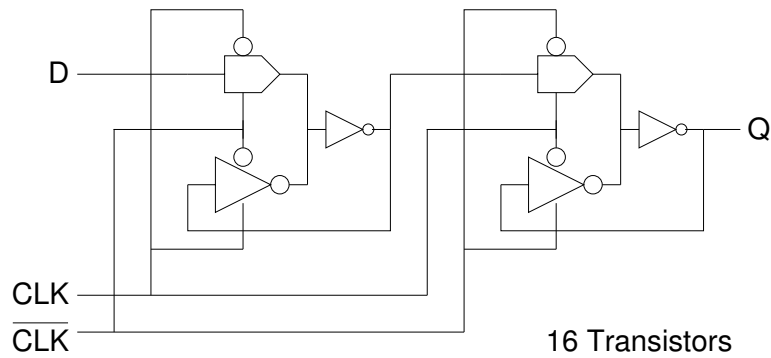
– Implementation



# Latches and Flip-Flops

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- Layout of master slave D type.

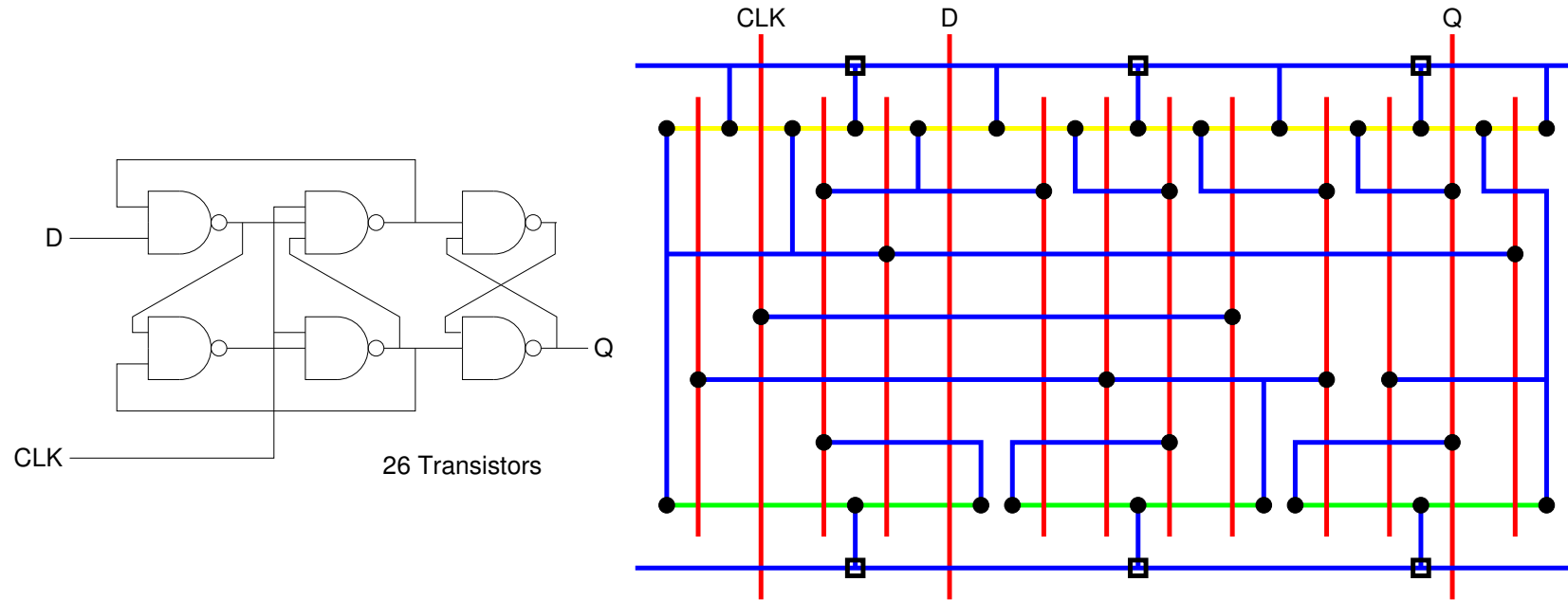


– very compact using alternative configuration.

# Latches and Flip-Flops

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- For the same functionality we could use an edge triggered D type:



- a few more transistors
- more complex wiring
- simpler clock distribution



