Requirements

- Full chip constraints
  including constraints on input and output ports

- SystemVerilog wrapper for top-level module
  including pad instances

- Chip pinout definition file
  in Encounter **.io** format

Full chip constraints (1)

- Specify Clock Frequency

```
create_clock -period 20 -name master_clock [get_ports Clock]
```

- Model Clock Tree *uncertainty = skew + jitter*

```
set_clock_latency     2.5 [get_clocks master_clock]
set_clock_transition  0.5 [get_clocks master_clock]
set_clock_uncertainty 1.0 [get_clocks master_clock]
```

- Specify Input and Output Timing

```
set_output_delay 2.0 -max -network_latency_included -clock master_clock \
    [all_outputs]
set_output_delay 0.1 -min -network_latency_included -clock master_clock \
    [all_outputs]

set_input_delay  2.0 -max -network_latency_included -clock master_clock \
    [remove_from_collection [all_inputs] [get_ports Clock]]
set_input_delay  0.1 -min -network_latency_included -clock master_clock \
    [remove_from_collection [all_inputs] [get_ports Clock]]
```

Full chip constraints (2)

- Specify Input Drive and Output Load

```
set_load 1.0  -max [all_outputs]
set_load 0.01 -min [all_outputs]

set_driving_cell -max -library c35_IOLIB_WC -lib_cell BU24P -pin PAD [all_inputs]
set_driving_cell -min -library c35_IOLIB_WC -lib_cell BU1P  -pin PAD [all_inputs]
```

- Specify Timing Exclusions

```
set_ideal_network [get_ports nReset]
```

- Other constraints

```
set_max_area 0
```

Full Chip Synthesis

Both **SystemVerilog Wrapper** and **Pinout Definition File** can be generated from a single source - e.g. `qmults_pads.txt` :

```
WRAPPER   wrap_qmults
CORE      qmults
INSTANCE  core_inst

TOP    INPUT       i_multiplicand[0]
TOP    PADS_VDD
TOP    INPUT       i_multiplicand[1]

LEFT   INPUT_CLOCK i_clk
LEFT   CORE_VDD
LEFT   OUTPUT      o_complete

BOTTOM INPUT       i_multiplier[1]
BOTTOM PADS_GND
BOTTOM INPUT       i_multiplier[0]

RIGHT  OUTPUT      o_result_out[0]
RIGHT  CORE_GND
RIGHT  OUTPUT      o_result_out[1]
```

Full Chip Synthesis

Run the command:

```
process_pad_ring qmults_pads.txt
```

to create:

1. **SystemVerilog Wrapper** : `wrap_qmults.sv`

```
module wrap_qmults (  input i_clk, .... );
...
  ICCK2P PAD_i_clk ( .PAD(i_clk), .Y(CORE_i_clk) );
...
  qmults core_inst ( .i_clk(CORE_i_clk), ... );
...
endmodule
```

2. **Pinout Definition File** : `wrap_qmults.io`

```
... (inst   name = "PAD_i_clk"    cell = "ICCK2P" ) ...
... (inst   name = "CORE_VDD_1"   cell = "VDD3IP" ) ...
```