ELEC6027 VLSI Design Project

Task:

Design and Implement a Novel 16-bit Microprocessor in $0.35\mu m$ CMOS (C035U)

- Complete IC Design Flow
- Complex System
  - Importance of Systematic Approach
  - Modular Design & Test
  - Manage Complexity through Hierarchy
- Team Exercise

ELEC6027 VLSI Design Project Milestones

1. Research Document — WED week 4 (19^{th} February 2014)
   - Report on Preliminary Research
2. Initial Design — WED week 5 (26^{th} Feb 2014)
   - Instruction Set, Datapath Diagram
3. Behavioural Model — WED week 6 (5^{th} March 2014)
   - SystemVerilog
4. Cross Simulation — WED week 7 (12^{th} March 2014)
   - SystemVerilog Control Unit, Magic Datapath
5. Final Design — FRI week 10 (2^{nd} May 2014)
   - Full Magic Design, Programmer's Guide
6. Project Report — Tue week 12 (13^{th} May 2014)
   - Report on Design and Implementation

Initial Design

Instruction Set

ADD

Syntax

`ADD Ry, Rz, Rx`

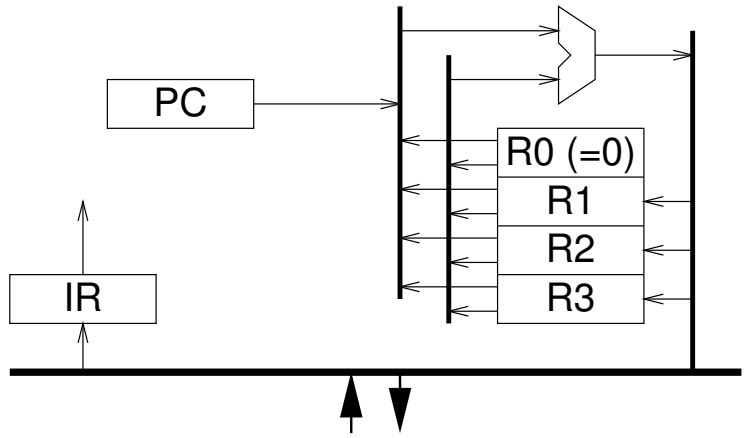
Semantics

Rx <- Ry + Rz

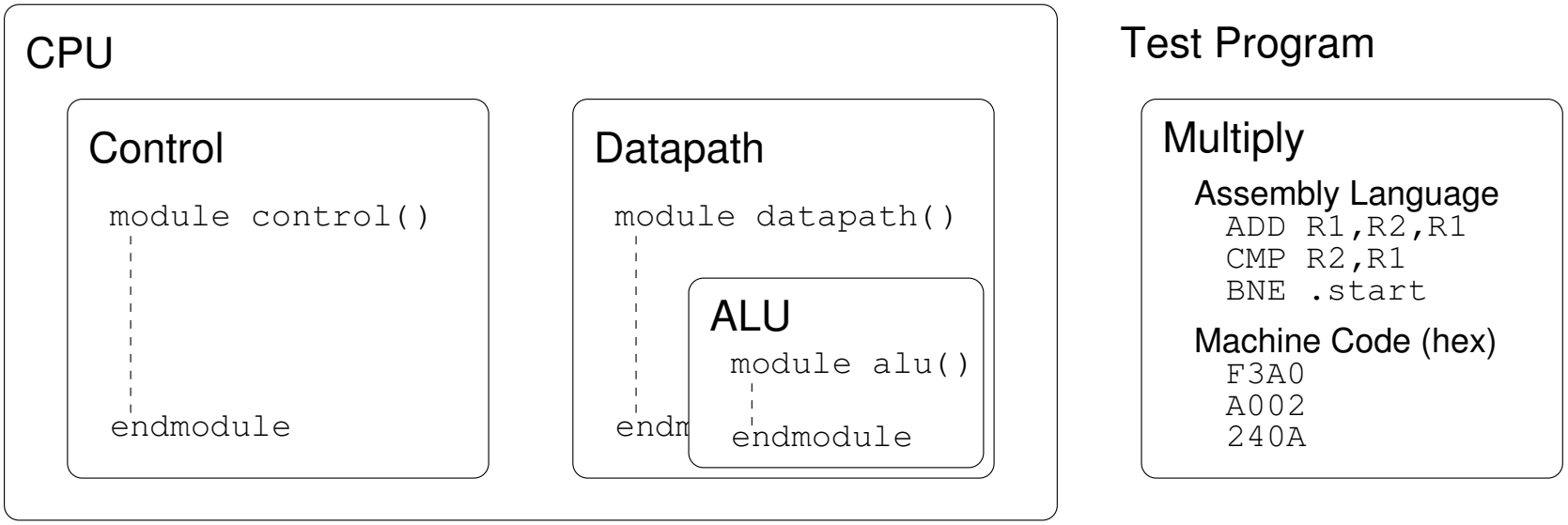
Coding

1011011	x	y	z

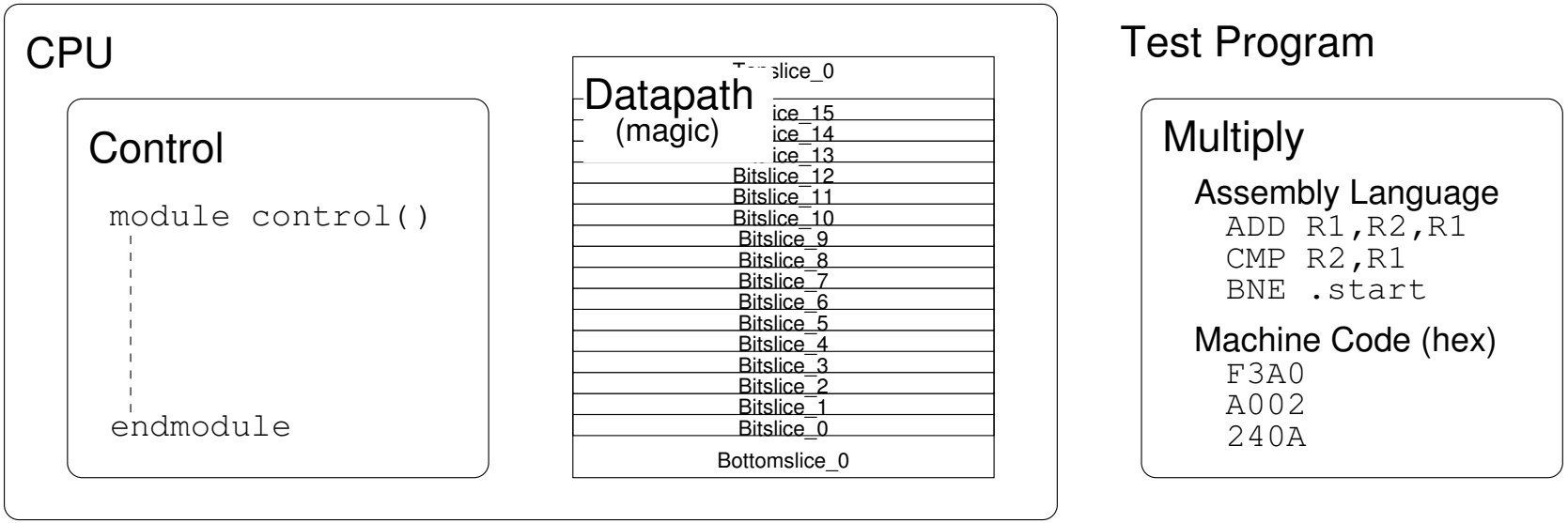
Datapath Diagram



Behavioural Model

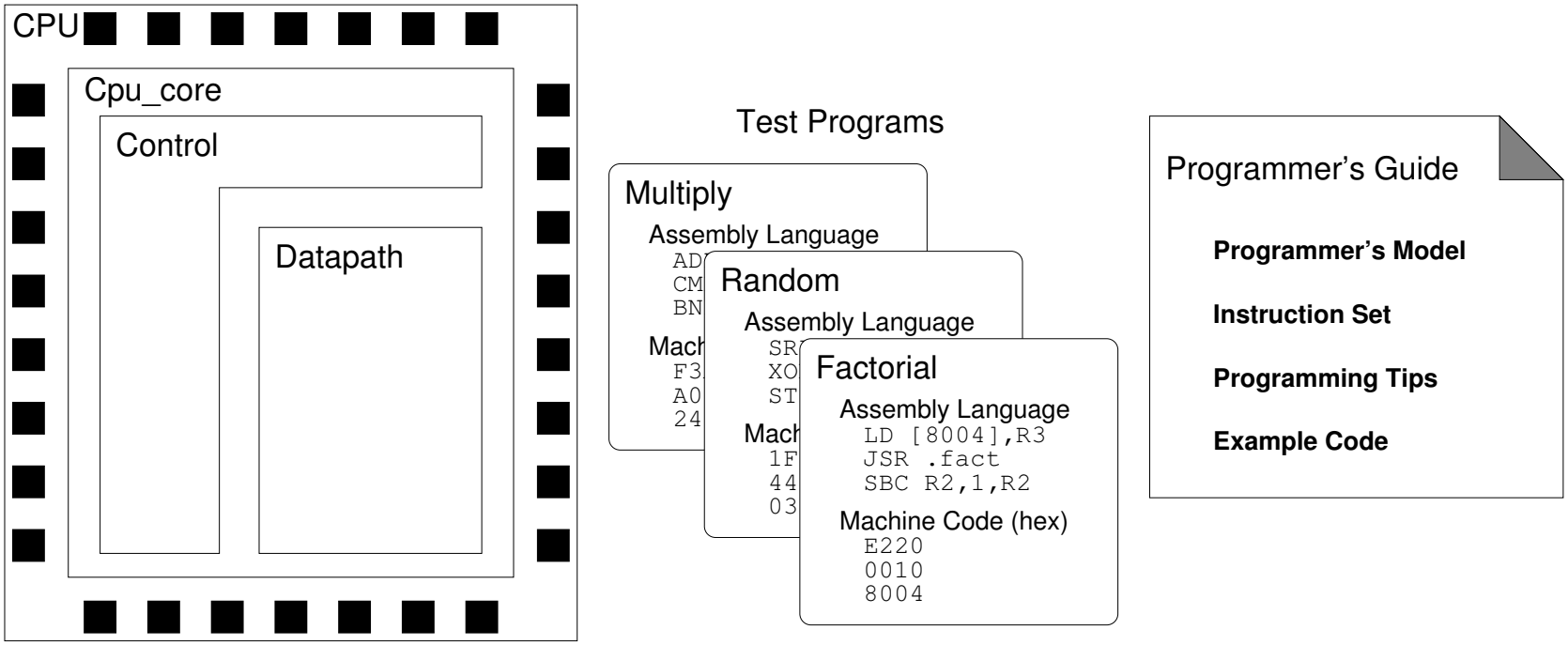


Cross Simulation



The submitted SystemVerilog control module may well be a newer version than that submitted with the behavioural model, in which case a newer SystemVerilog datapath module must also be submitted.

Final Design



An updated SystemVerilog behavioural model of the processor must be submitted with the final design.

week	MON	TUE	WED	THU	mini milestones	FRI
1				LAB	Confirm Teams	
2				LAB	Declaration of Specialisms	
3				LAB	*t.b.a.*	
4			**Research Report**	LAB	Draft Design	
5			**Initial Design**	LAB	Initial Behavioural Model (executes at least 4 instructions)	
6			**Behavioural Model**	LAB	Simulation of Basic Datapath (including ALU and Data Registers)	*Behavioural Model with Interrupts*
7			**Cross Simulation**	LAB	Simulation of Placed and Routed Control Unit	
8				LAB	*t.b.a.*	
9				LAB	Simulation of First Cut Chip in Pad Ring	
10				LAB	*t.b.a.*	**Final Design**
11				—		
12		**Project Report**				

ELEC6027 VLSI Design Project Thursday Lectures

Week	Time	Topic
1	10:00	**Introduction** *This lecture*
2	10:00	**Basic Processor Design** *Including RISCish and CISCish examples*
3	10:00	**Processor Datapath Design** *Including RISCish and CISCish example*
4	10:00	**Behavioural Modelling** *This seminar is intended for SystemVerilog specialists only*
5	10:00	**Advanced Bitslice Design** *This seminar is intended for Datapath specialists only*