

VLSI

VLSI Systems Design

Iain McNally

< 12 lectures - Monday(?) Afternoons¹

+15 Theory Lectures *for MSc Students*

12 lab sessions - **Every Thursday Afternoon**

+ occasional extra lab sessions?

¹lectures advertised via the course e-mail list

VLSI Systems Design

- Content

- Layout for VLSI

- Cell layout, Standard cell layout, Full and semi-custom design, Floorplanning, Bit slice design.

- Digital design using SystemVerilog

- Introduction to SystemVerilog, Design for Synthesis.

- CAD Tools & Techniques

- Magic VLSI layout editor, HSpice analogue circuit simulator, SystemVerilog Hardware Description Language and digital simulator, Cadence IC design toolset.

VLSI Systems Design

- **Assessment - 100% Coursework**

Desex1 10% Design and optimization of a CMOS gate using Magic

Mini design exercise – automatically marked – No formal write-up

Desex2 10% Design of a digital system using SystemVerilog HDL

Mini design exercise – No formal write-up

Desex3 40% Design of a standard cell library using Magic

Team exercise – Formal report

Desex4 40% Bitslice Design using Magic and SystemVerilog HDL

Individual exercise – Basic documentation (just design diagrams)

Assess 25% Ongoing laboratory assessment

Attendance + Progress + Up to date log book

+ Mask-Level Layout Exercise *for MSc Students*

$$\text{Mark} = (\text{Desex1} + \text{Desex2} + \text{Desex3} + \text{Desex4}) \times \frac{75 + \text{Assess}}{100}$$

VLSI Systems Design

- **Book**

- **Integrated Circuit Design**

- a.k.a. Principles of CMOS VLSI Design - A Circuits and Systems Perspective

- Neil Weste & David Harris

- Pearson 2011

- **Notes & Resources**

- Lecture notes and Design Exercises

- <http://secure.ecs.soton.ac.uk/module/ELEC6230/>

- Lab Sheets and Reference Material

- <http://secure.ecs.soton.ac.uk/notes/bim/notes/cad/>