

CHAPTER 7

THE DIGITAL ACCELEROMETER

7.1 Basic Considerations

As outlined in Chapter 6 an analogue, closed loop accelerometer has some inherent disadvantages such as the nonlinear feedback relationship and consequent stability problems for large deflections of the seismic mass. It is intended in this chapter to show that it is not only possible to solve these problems but to design an inherently digital accelerometer which would use a different feedback strategy. Such a device would lend itself to inclusion in large-volume, low-cost systems taking advantage of digital data processing, Cole and Braun [19].

Recently the Nonlinear Systems Design Group at Coventry University has developed a range of digital transducer prototypes for example a power transducer, Lewis et. al. [59], a current transducer, Lewis and Hesketh [58], and a digital weighing machine, Lewis et. al. [60]; all rely on a special form of oversampling technique or sigma-delta modulation for their operation. Before describing the digital transducer concept it is necessary to consider the modulator structure.

7.1.1 Sigma-delta Modulator

A typical, first order sigma-delta modulator, fig. 6.1, is a type one, closed loop system having the important property of a zero steady state error when subjected to a constant input signal. $G_L(s)$ represents the transfer function of the linear components in the forward path incorporating one free integrator. This is followed by a sampled comparator with a sampling period ' T_s '. The output signal from the comparator can be interpreted as a digital signal and constitutes the output signal

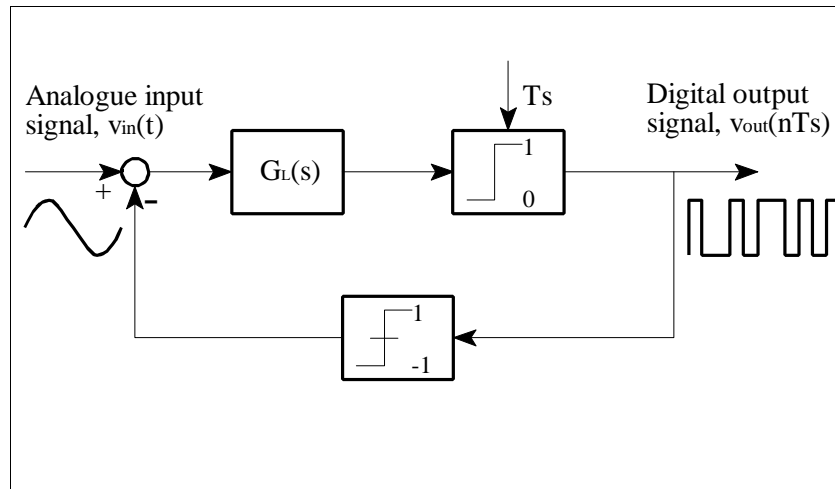


Fig. 7.1: First order sigma-delta modulator.

of the modulator which is a pulse density modulated bitstream. As the signal is unipolar a one bit digital to analogue converter (DAC) is required in the feedback path to convert the output signal to bipolar format. As a result of the system dynamics the system oscillates continuously in the unforced condition in one or more limit cycle modes, Lewis [55], which are locked to the clock signal frequency. In the case of a single valued symmetrical nonlinearity in a type one system the limit cycle period in the unforced condition is symmetrical about zero which is realized by a mode having a period of $2nT_s$, where n is a positive integer and designates the number of samples per half-cycle of the input signal to the clocked comparator. The usual notation is to refer to the limit cycle as an (n,n) mode. The limit cycle, in effect, acts as a carrier signal for the analogue input signal.

The principle of operation of a sigma-delta modulator relies on the fact that the sampling frequency is much higher than the frequency of the analogue input signal, hence sigma-delta modulators are also called oversampling converters. The ratio between the sampling frequency and the highest frequency component of the input signal is usually referred to as the oversampling ratio. As a result of the oversampling process the average of the output bitstream is a measure of the input signal $v_{in}(t)$. In the frequency domain the pulse density modulated bitstream comprises a component of the input signal and some quantization noise which is swept out of the signal band by the oversampling process, Candy and Temes [17]; this is considered briefly in Appendix II. The quantization noise may be removed by a low-pass filter which is typically realized by a decimation filter converting the serial bitstream into an n -bit parallel signal, Candy [16].

Sigma-delta modulators have application in the telecommunication and audio industries as a means of A to D conversion, especially for high accuracy. High order modulators, employed to obtain an improved signal to noise ratio, contain more than one energy storage element, Ferguson et. al. [28]. However, due to the high order, such systems may only be conditionally stable and may exhibit complex orbits in the phase space, Littlehales [69], Agrawal and Shenoi [1], hence such devices are more difficult to stabilize and implement in hardware. Consequently for the application of a sigma-delta modulator to interface with a sensor only a first order modulator was considered.

In recent years sigma-delta modulators have attracted a wealth of research. Most of the work is concerned with the noise shaping characteristics of different system structures, the analysis of quantisation noise, system architecture and stability. The work described here should not be seen as a contribution towards sigma-delta modulator related research; it merely uses the modulator as a vehicle for the design of a digital transducer.

7.1.2 Digital Transducer Concept

Instead of using a sigma-delta modulator to convert the analogue output signal from a sensor to the digital domain, Spangler and Kemp [91], it is possible to use a sigma-delta modulator structure to realise an inherently digital, closed loop transducer; fig. 7.2 shows the generic digital

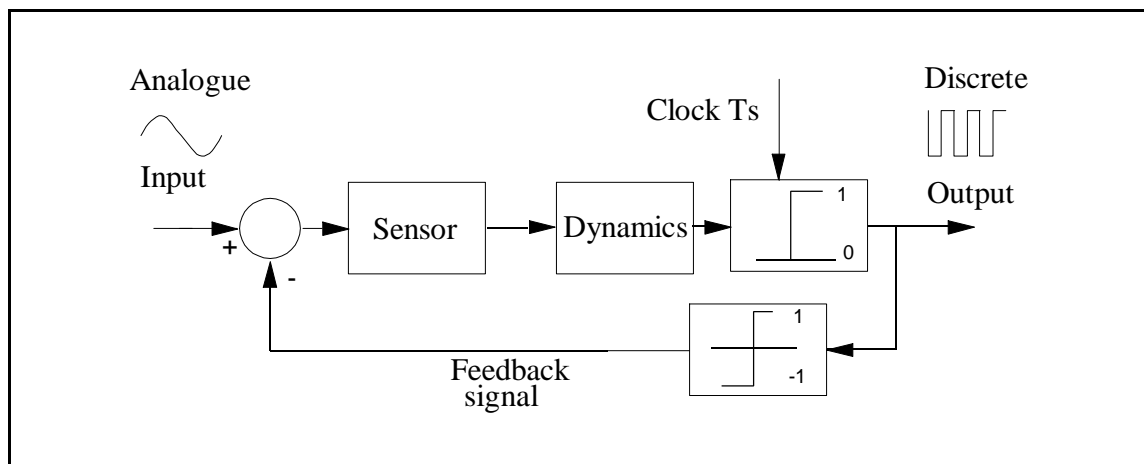


Fig. 7.2: Digital transducer structure.

transducer concept. The sensing element is included in the forward path of the modulator. Basic considerations of the application of such an approach to an accelerometer are discussed in Lewis et. al. [62].

The common properties of any digital transducer are described below:

- < The output signal is directly digital and suitable to interface with standard digital equipment such as a digital bus system or a computer. There is no need for a separate ADC. This is especially advantageous in electrically noisy environments such as automotive applications since a digital signal is robust and has higher noise immunity than an analogue signal. The digital signal can be easily processed using powerful DSP algorithm, e.g. if the accelerometer is used to provide a measure of velocity and position it is much easier to integrate the digital signal since analogue integration always suffers from problems caused by drift and subsequent saturation effects, Kraft et. al. [46].
- < If several transducers transmit data to a central host computer, the digital signals can be readily and cheaply multiplexed.
- < Sigma-delta modulators lend themselves to VLSI implementation. In the case of a micromachined, digital accelerometer, the entire transducer could be integrated on one silicon chip.
- < A digital transducer exhibits a flat frequency response from d.c. to a frequency determined by the sensor dynamics and the control electronics.
- < Such a sensor, similar to a typical sigma-delta modulator, exhibits a limit cycle which may be used for self-testing purposes. In the case of an accelerometer this is especially important e.g. if the sensor is used to trigger off the release of an airbag. In such an application the sensor can be dormant for years but has to work reliably on the one occasion.

- < A trade-off between accuracy and bandwidth is possible, this means that it is possible to tailor the bandwidth - accuracy product to the application.
- < It can be shown that this type of limit cycling system is self-adaptive - it adapts itself to component tolerances, Lewis and Zikic [57] - which are always present when realising a system in hardware.

The dynamics of the sensing element in the forward path obviously increases the order of the system and therefore special attention must be paid to the stability of the closed loop system, consequently compensation may be required, e.g. Lewis and Crump [61] suggest PID compensation for digital transducers.

In the following sections the application of such an approach to the micromachined sensing element supplied by Druck Ltd. will be described. Digital accelerometers based upon similar system strategies have been reported by Yun et. al. [113], Henrion et. al. [38], Smith et. al. [89,90], Wuestling et. al. [112], Spinneau et. al. [92] and Fedder and Howe [27], however, in these papers little attention has been paid towards the control system design or the derivation of a mathematical model.

7.2 Principle of Operation

The application of the digital transducer control strategy to the accelerometer is illustrated in the block diagram of fig. 7.3.

In the forward path the mathematical model of the sensing element is used in its linearized form, small deflections of the seismic mass being assumed. The measurement of the position of the mass is assumed to be a simple gain block (for the digital accelerometer a different pick-off circuit had to be designed which is discussed in sec. 7.4). The action of the sampled comparator can be modelled by a sampler followed by an ideal relay. The two logic states of the comparator correspond to a positive or negative imbalance in capacitance of the sensing element and can be

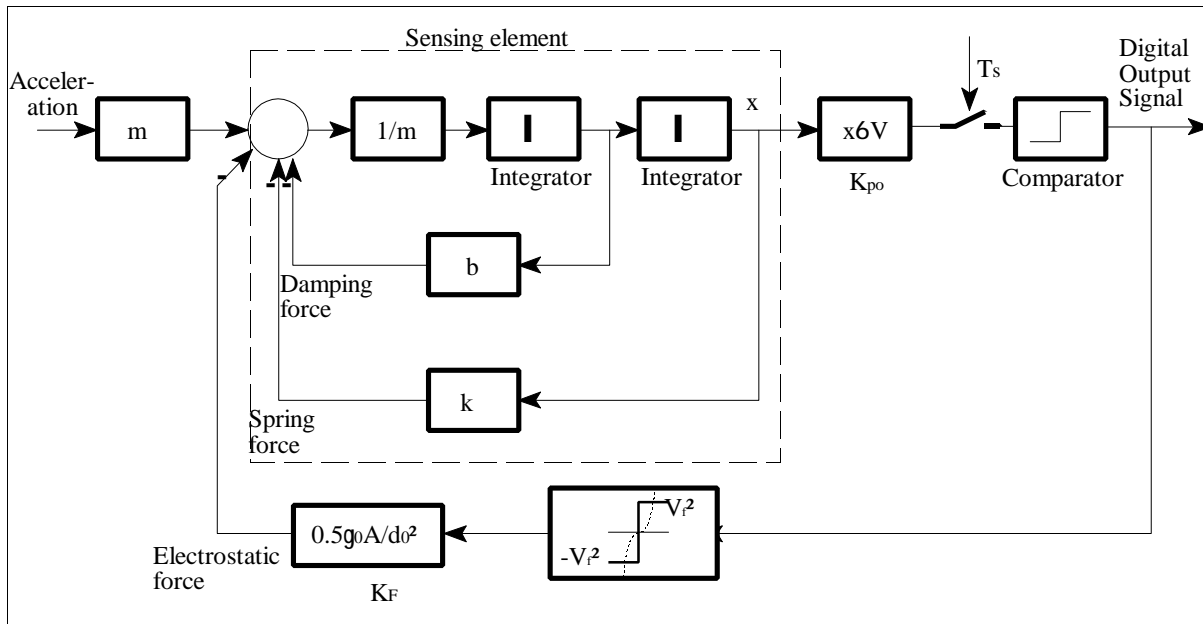


Fig. 7.3: Fundamental system structure of a digital accelerometer.

interpreted as the seismic mass being above or below the central position between the electrodes. By investigating the structure shown in fig. 7.2 it can be seen that the feedback signal is generated by a clocked comparator and a one bit DAC, consequently it consists of pulses of constant magnitude and duration which is determined by the sampling frequency of the system. In the case of the accelerometer this can be achieved by applying a pulse of voltage to the electrode furthest from the seismic mass, the other electrode being grounded. The electrode which is energized is determined by the logic state of the comparator. In this way only one electrostatic force is generated on the seismic mass which pulls it back to the central position, thus negative feedback action is produced even though the forces employed are always attractive; at first glance a very surprising fact.

As the magnitude of the voltage pulse is constant the magnitude of the electrostatic force is also constant; the nonlinear relationship between voltage and force, which is the reason for an inherently nonlinear feedback relationship for the analogue, closed loop accelerometer, has been fixed to two possible values with equal magnitude but of opposite polarity (providing the seismic mass stays very close to the central position). The average feedback force can now be assumed to be a linear function of the number of pulses in force over a certain time interval.

At this stage it also becomes obvious that such a system must have a superior stability compared to the analogue, closed loop accelerometer, since a voltage is only applied to one electrode at a time, the difficult task of balancing two electrostatic forces, as in the analogue, closed loop system, does not need to be considered anymore. Furthermore, because the sampling frequency is much higher than the signal frequency, the duration of a voltage pulse applied to one electrode is much shorter than the time constant of the sensing element hence the overshoot of the seismic mass above its rest position is negligible, consequently a ‘latch up’ is not possible.

As for a sigma-delta modulator it is to be expected that a digital accelerometer would exhibit a stable limit cycle in the quiescent state; this can be demonstrated as follows: assuming that the comparator is in a defined state then a voltage will be applied to one electrode causing the seismic mass to be attracted towards it; the pick-off circuit will detect this movement and consequently the comparator will change its polarity after the next sampling action. The feedback voltage, ‘ V_F ’, is then applied to the opposite electrode and the cycle recommences.

The above propositions have been investigated further and verified by simulation and laboratory measurements presented later in this chapter.

7.3 Theoretical Analysis

The analysis presented in this work relies upon the application of describing function theory, Gelb and Van der Velde [32]. With this mathematical tool possible limit cycling modes for the unforced condition and their stability can be predicted. Use of the multiple input describing function enables the prediction of the closed loop performance to be undertaken. In this analysis the linearized transfer function of the sensing element is used, thus making again the assumption that the seismic mass stays close to the central position.

7.3.1 Limit Cycle Prediction

Describing function analysis is justified in this case, as the accuracy of the approach relies on the

attenuation of higher harmonic components produced by the nonlinearity in the system; since the sensing element effectively represents a mechanical low pass filter a significant high frequency attenuation can be assumed. The clocked comparator can be modelled as a series combination of a sampler, a zero order hold (z.o.h.) and an ideal relay as shown in fig. 7.4. Since the nonlinearity is single valued it is permissible to rearrange the order of the series combination of components, Lewis [55], to facilitate the prediction of limit cycles.

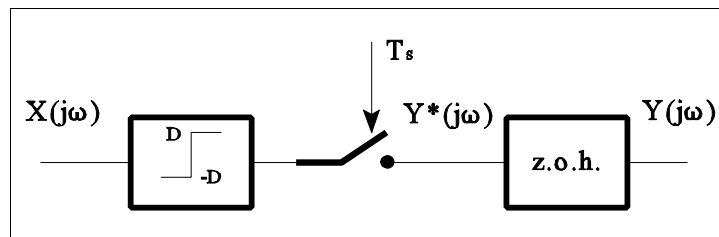


Fig. 7.4: The nonlinear component of the digital accelerometer represented in a manner suitable for mathematical analysis.

The sinusoidal input describing function for the relay, sampler and z.o.h. combination has the form, Lewis [56]:

$$N(P,M) = \frac{4D}{\pi B} e^{jM} \quad \dots(7.1)$$

where ‘D’ is the operating level of the relay, ‘P’ the magnitude of the sinusoidal input signal to the nonlinearity combination and ‘M’ is the lagging angle introduced by the sampling action for which a possible range can be determined depending on the mode of oscillation as shown in table 7.1.

Limit cycle mode (n,n)	Lagging angle M
(1,1)	M ∈ [0, B]

(2,2)	M O [0, B/2]
(3,3)	M O [0, B/3]
(4,4)	M O [0, B/4]
(n,n)	M O [0, B/n]

Table 7.1: Possible phase shift introduced by the sampling process.

With this representation of the nonlinearities it is possible to obtain a mathematical model of the digital accelerometer as illustrated in fig. 7.5 in which the feedback gain of the system is again abbreviated as ‘K_F’, the gain of the pick-off circuit as ‘K_{po}’.

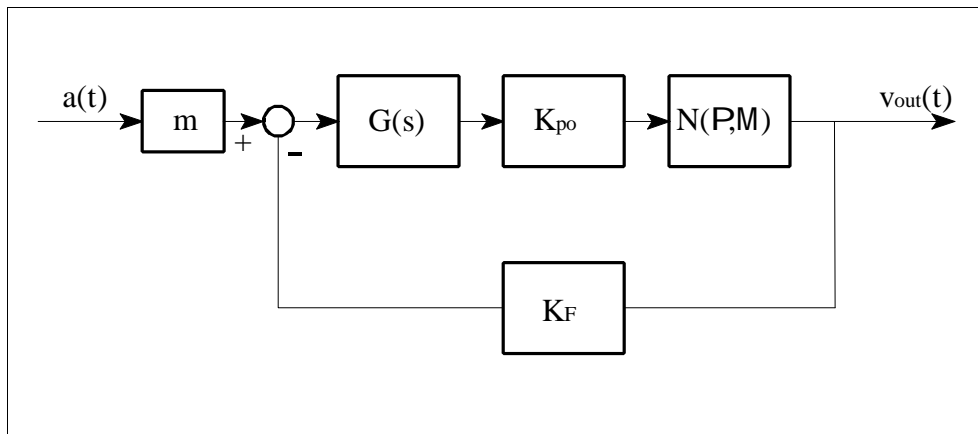


Fig. 7.5: Mathematical representation of the digital accelerometer.

To predict possible limit cycling modes the solutions to the system characteristic equation

$$1 + K_{po} K_F G(jT) N(P,M) = 0 \quad \dots(7.2)$$

must be determined.

For the digital accelerometer the characteristic equation has the form:

$$1 - K_{po}K_F \frac{1}{m(jT)^2 + bjT + k} \frac{4D}{BK_{po}X} e^{sT} = 0 \quad \dots(7.3)$$

where the sinusoidal input to the nonlinearity, 'P', was expressed with respect to the amplitude of the movement of the seismic mass, $X = K_{po}P$. Eq.(7.3) can be solved graphically, in which the linear transfer function is presented as an inverse polar plot. In this type of system, due to symmetry, the limit cycle frequency is an integer multiple of the sampling frequency, therefore $1/G(jT)$ need only be calculated at $T = 2Bfs/2n$, Lewis [56]; the highest frequency limit cycling mode contains one sample per half cycle and is referred to as a (1,1) mode hence the frequency is equivalent to half the sampling frequency.

In fig. 7.6 the graphical solution for the characteristic equation is shown with the parameters of the articulated sensing element, a sampling frequency of 10 kHz, a feedback voltage on the electrodes of $V_F = 40$ V and a pick-off circuit gain of 1.6 V/ μ m. It is obvious that (1,1) and (2,2)

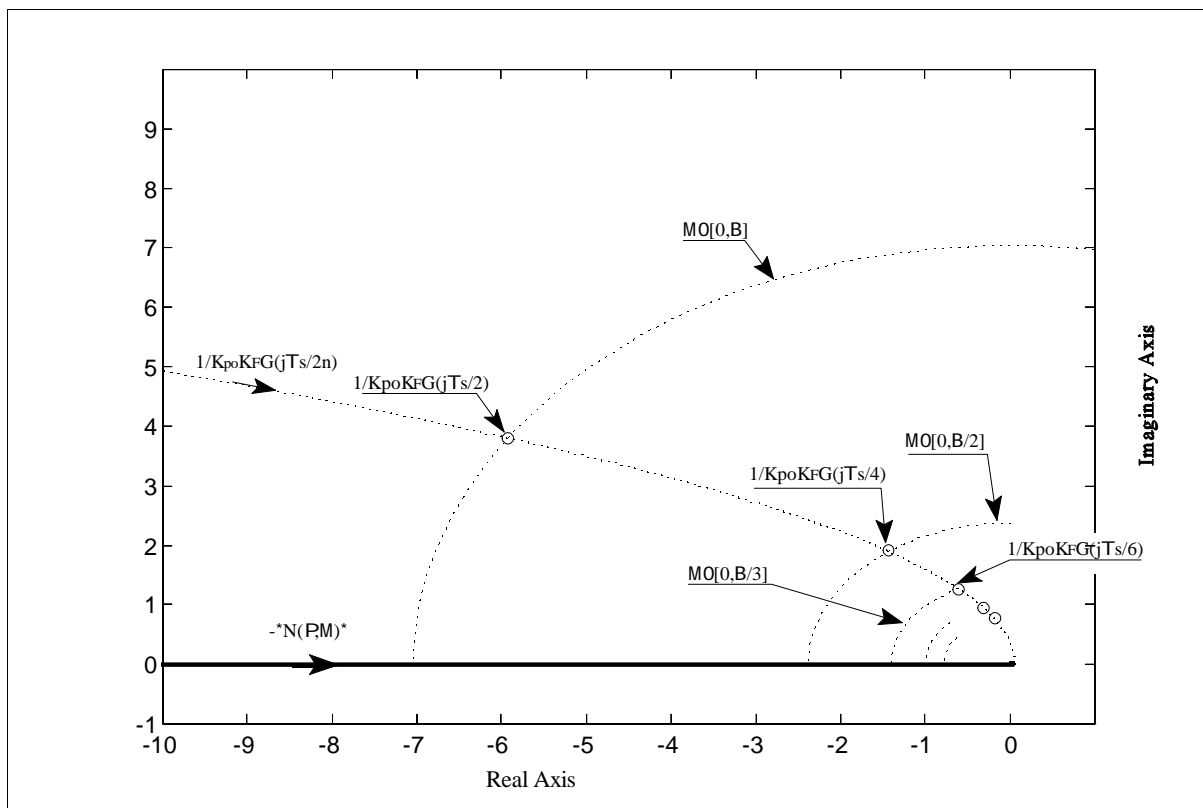


Fig. 7.6: Graphical solution of the characteristic equation for the mathematical model of the digital accelerometer.

modes are possible since the phase shift introduced by the sampling action is large enough to make an intersection of $1/G(j2Bf_s/2n)$ and $N(X,M)$ possible. A (3,3) mode is also possible, however, the phase margin is very small as the phase shift of $1/G(j2Bf_s/6)$ is 135.68° , hence this point lies only 0.68° inside the segment representing the maximum phase shift introduced by the sampling action. However, it is doubtful whether such an accuracy can be expected from the analysis since the describing function is an approximate method and additional simplifications had to be made to derive the mathematical model for the digital accelerometer.

By solving eq.(7.3) at the possible limit cycle modes an expression to predict the magnitude of the displacement of the seismic mass, 'X', can be found:

$$X = \frac{4DK_F * G(jT_s / 2n)^*}{B} \quad \dots(7.4)$$

'X' was calculated as 0.11, 0.34 and 0.57 μm for (1,1), (2,2) and (3,3) modes respectively. In order to justify the assumption that the electrostatic force does not depend on the movement of the seismic mass, 'X', should be keep as small as possible. From eq. (7.4) it can be seen that 'X' increases with the feedback gain but decreases for either low limit cycle modes and high sampling rates since $*G(jT_s/2n)^*$ decreases with increase in 'n' or 'T_s'.

The above findings were verified by simulation in Matlab/SIMULINK. The SIMULINK

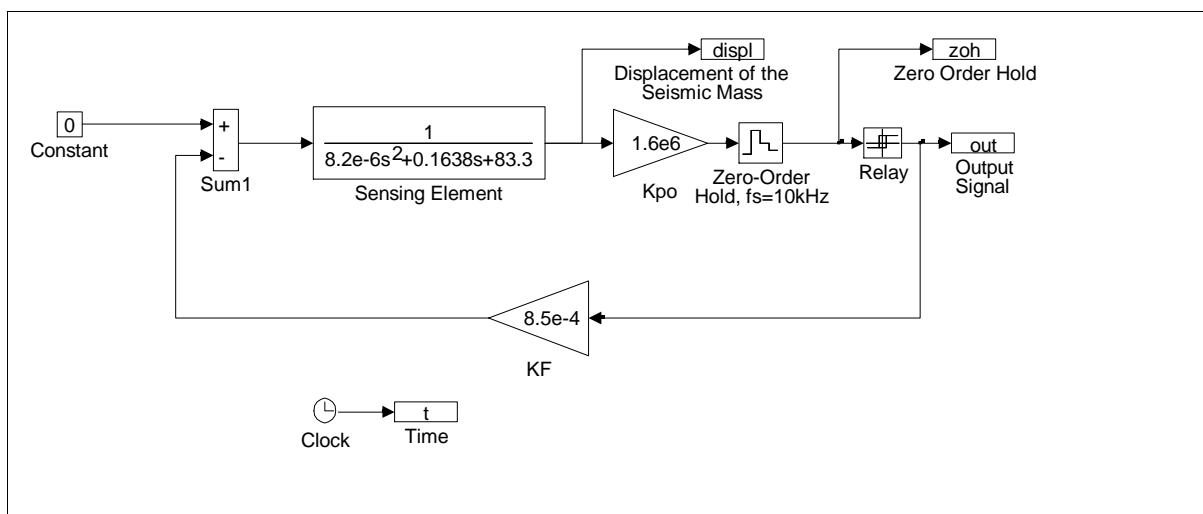


Fig. 7.7 SIMULINK model used to verify the describing function analysis.

simulation model is depicted in fig. 7.7. Although several integration methods were tried the only limit cycle exhibited was a (2,2) mode indicated by the two samples per half cycle. The top trace of Fig. 7.8 shows the displacement of the seismic mass and the z.o.h. output signal which was scaled to an appropriate range by dividing it by 'K_{po}'. The waveform of the movement of the seismic mass is a good approximation to a sinusoid, hence enough filtering of higher frequency components introduced by the relay is achieved. The peak values found by simulation of the movement was 0.35 μm which agreed well with the value predicted theoretically. The bottom trace shows the output signal of the relay.

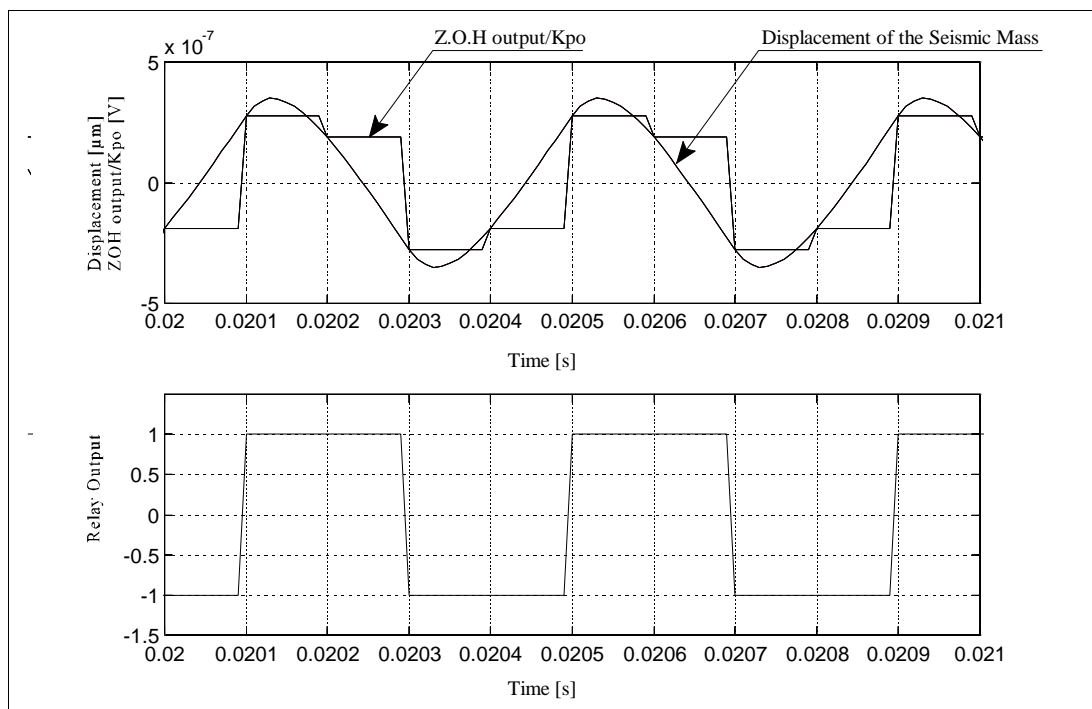


Fig. 7.8: Simulation result showing a (2,2) mode. The top trace shows the movement of the seismic mass and the output of the zero-order-hold divided by 'K_{po}'; the bottom trace shows the output of the relay.

For accurate coding it may be necessary to introduce some form of compensation. In this regard a PI-controller was considered (see section 7.3.3). Since the limit cycle frequency is high and if the integral gain, $K_I \neq K_P$ the influence of the integral gain may be neglected in the limit cycle prediction. Consequently, the inverse polar plot of the open loop linear transfer function shown in fig. 7.6 is not altered and therefore the limit cycle modes are unchanged. In fact, it was found by simulation that a (2,2) mode with approximately the same mass movement could be assumed

up to a ratio of $K_I/K_P < 1000$. However, if the integral gain is even larger or, in the extreme case, $K_P = 0$ its effect obviously cannot be neglected. The inverse polar plot lies in the second quadrant only for low frequencies, hence only high order limit cycle modes are possible. Fig. 7.9 shows the situation where pure integral gain, $K_I = 1$, was assumed, the linear part of the system is abbreviated with:

$$G_L(s) = G(s) K_{po} K_F \frac{K_I}{s} \quad \dots(7.5)$$

An intersection between $1/G_L(j2Bf_s/2n)$ and $N(X,M)$ is possible for (10,10) to (16,16) modes. The displacement magnitude varies from 2.1 μm to 3.3 μm . This was confirmed by simulation where a (14,14) mode with a displacement magnitude of 3.5 μm was observed. It is obvious that such a large movement of the seismic mass violates the assumption that the electrostatic force is independent of the motion. Consequently, a ‘classical’ sigma-delta modulator structure, with a pure integrator in the forward path, cannot be used for the design of this transducer. A

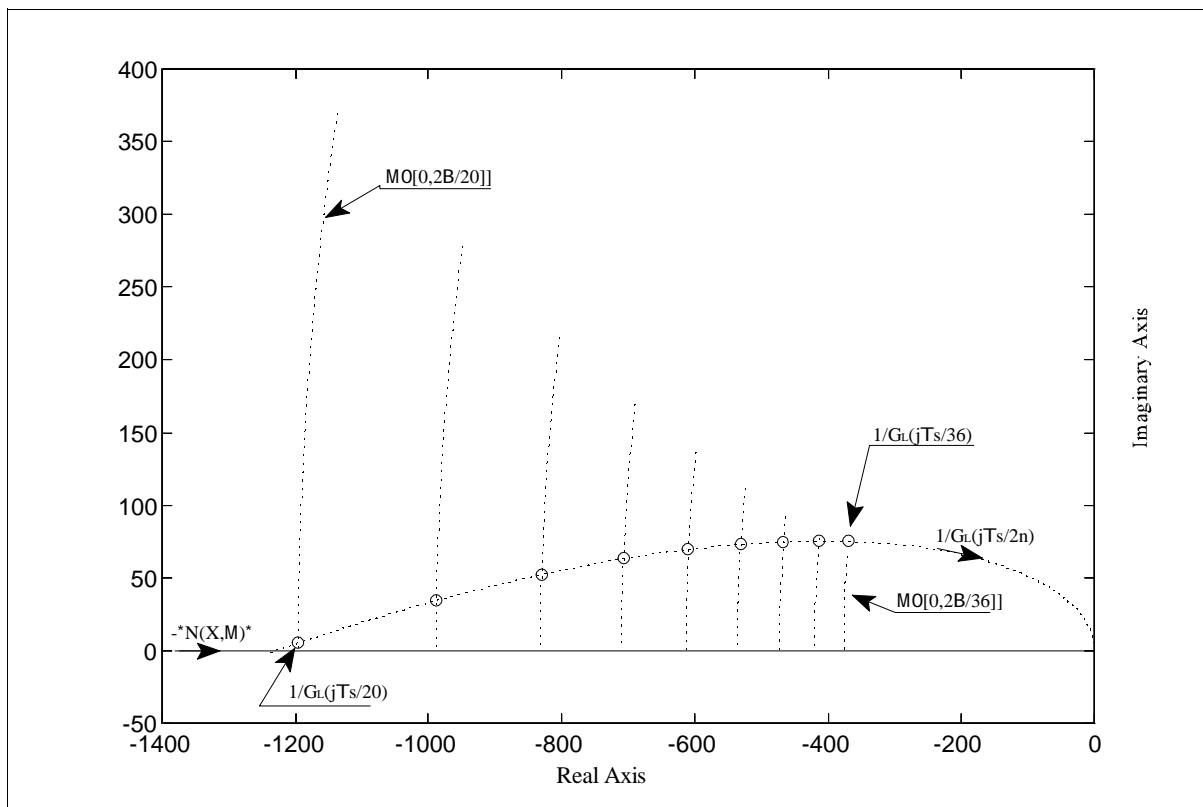


Fig. 7.9: Limit cycle prediction for a pure integral gain in the forward path. Modes between (10,10) and (16,16) are possible.

proportional gain component is required to ensure a low order mode limit cycle. The choice of the values for K_P and K_I will be discussed further in sec. 7.3.3.

7.3.2 Performance Prediction

Up to this point the accelerometer was considered to be unforced. In order to predict the closed loop performance the effect of an input acceleration had to be investigated. It was stated earlier that the maximum frequency of the input acceleration is below 300 Hz; hence it can be considered to be equivalent to a quasi-stationary (or bias) signal, 'B', compared to the frequencies of (1,1) or (2,2) limit cycle modes which are 5 and 2.5 kHz respectively for a sampling frequency of 10 kHz. This is the requirement for the application of the dual-input describing function, where the gain of the nonlinearity to the input signal or bias component is described by $N_B(P,B)$ which is independent of the sampling angle since the phase shift introduced by the sampling action is negligible at these frequencies. The bias component of the dual input describing function for the relay and sample and hold combination has the general form:

$$N_B(P,B) = \frac{2D}{BB} \arcsin(B/P) \quad \dots(7.6)$$

For small acceleration magnitudes it is possible to make the further assumption that the magnitude of the bias signal caused by the input acceleration is small compared to the magnitude of the limit cycle. The range of input acceleration for which above statement is valid can be determined by the following consideration. As the input signal is required to be of low frequency the transfer function of the sensing element reduces to the steady state form which is m/k . The resultant deflection of the seismic mass, 'x', consists of two components, 'x_B' due to the input acceleration and 'x_{LC}' due to the limit cycle. If, as it is normally found in practice, $x_B \neq (1/3) \cdot x_{LC}$, then the incremental describing function may be employed, Gelb and Van der Velde, [32]. For example with a (2,2) limit cycle mode the maximum input acceleration, for which this condition is valid, can be found to be approximately 0.1 g. The dual input describing function bias component approximates to the incremental describing function $N_I(P)$:

$$N_I(P) \cdot N_B(P,B) \cdot \frac{2D}{BB} \arcsin(B/P) \cdot \lim_{B \rightarrow B_0} \frac{2D}{BP} \quad \dots(7.6)$$

This expression is independent of ‘B’, hence the nonlinearity represents a linear gain to the input signal. The closed loop mathematical model simplifies to the linear system as shown in fig. 7.10.

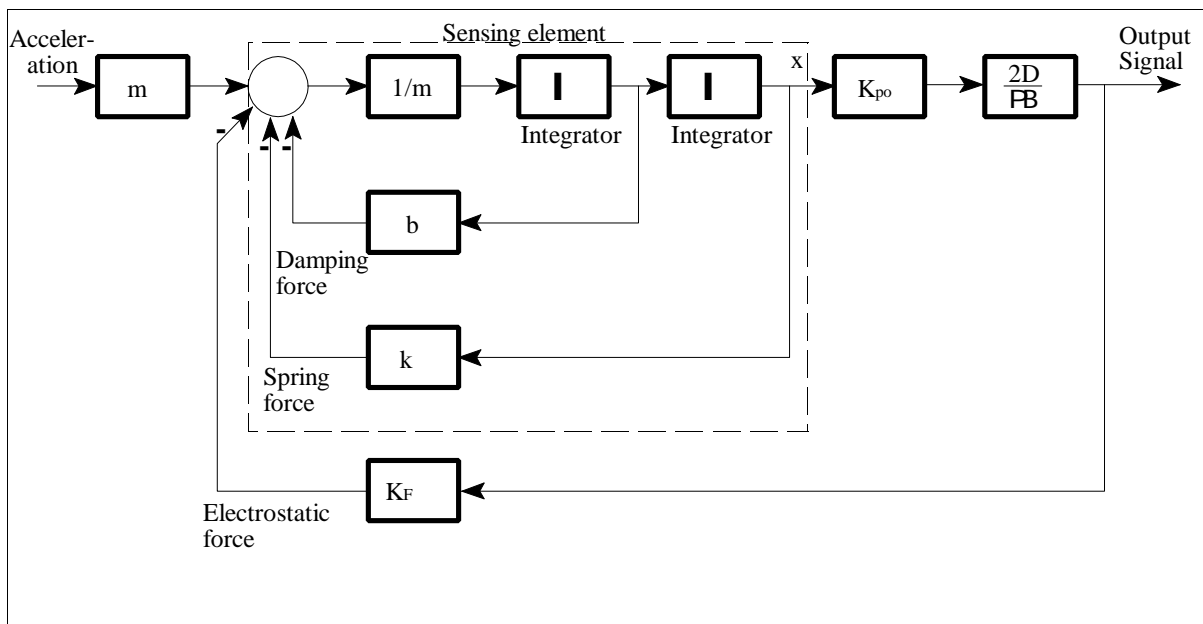


Fig. 7.10: Linearized mathematical model of the digital accelerometer derived by applying incremental describing function theory.

The closed loop transfer function of the digital accelerometer is given by eq. (7.7). It should be noted that it depends on the limit cycle mode and is independent of the gain of the pick-off circuit.

$$F_{cl}(s) \cdot 2Dm \frac{1}{mBs^2 + bBs + kBs + 2DK_F} \quad \dots(7.7)$$

The frequency response for a (1,1) mode for different feedback voltages, is shown in fig. 7.11 and for a (2,2) mode in fig. 7.12.

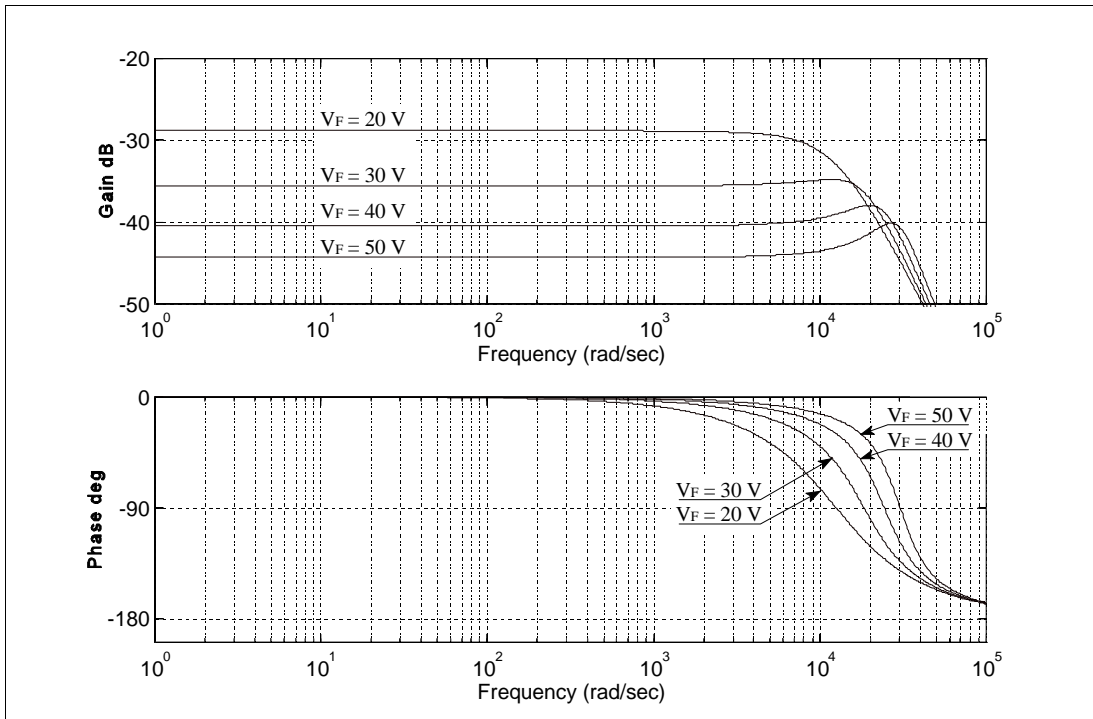


Fig. 7.11: Frequency response for a (1,1) mode and different feedback voltages.

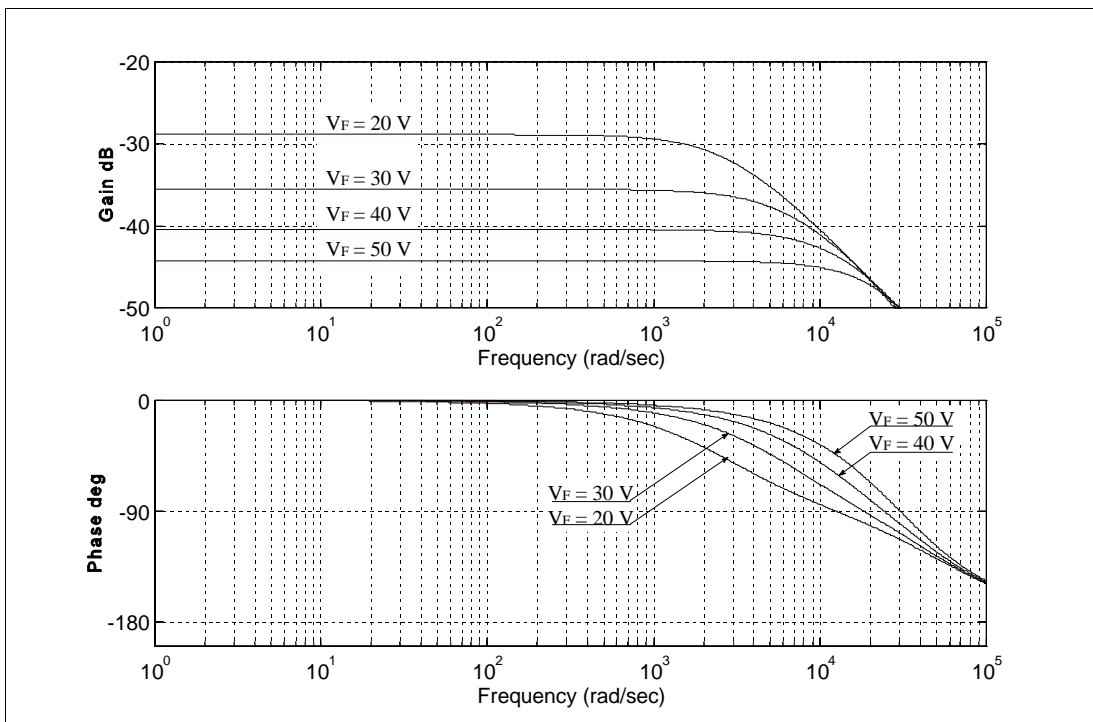


Fig. 7.12 Frequency response for a (2,2) mode and different feedback voltages.

Inspection of fig. 7.11 reveals that the -3 dB cut-off frequency lies in the range from 1.7 kHz for

$V_F = 20$ V to 3.3 kHz for $V_F = 50$ V; fig. 7.12 indicates cut-off frequencies between 440 Hz for $V_F = 20$ V to 3.2 kHz for $V_F = 50$ V. However, the correct interpretation of these values is of utmost importance. For such high cut-off frequencies the assumption made for this analysis, that the signal frequency caused by the input acceleration is much smaller than the frequency of the limit cycle, is certainly violated hence a correct prediction of the cut-off frequency of the digital analysis is not possible with this method. The benefit of the above analysis is that it is possible to predict certain tendencies:

- , for frequencies much smaller than the limit cycle frequency a flat frequency response and a linear transfer characteristic are expected;
- , the higher the sampling frequency, the higher the limit cycle frequency hence the higher the bandwidth of the transducer;
- , for higher limit cycle modes a lower cut-off frequency is expected;
- , an increase in feedback voltage results in an increase in bandwidth;

Similar to the limit cycle prediction the influence of a PI controller on the accelerometer performance was investigated. Unity proportional gain was chosen and the integral gain was assumed to lie in a magnitude range that the same modes and magnitudes of the movement of the seismic mass as without a controller can be expected. The small signal closed loop transfer function of the digital accelerometer has then the form:

$$F_{CL}(s) = \frac{2Dm K_I s}{m^2 B X_s^3 + b B X_s^2 + (k B X_s + 2DK_F)s + 2DK_F K_I} \quad \dots(7.8)$$

The frequency response for this transfer function using the same values for the feedback voltage is very similar to the one without the PI controller for both modes, hence from this analysis it is not expected that the PI controller has any significant effect on the transducer performance in terms of bandwidth or the flatness of the frequency response in the signal band.

7.3.3 Coding Accuracy

In this chapter the coding accuracy, especially the influence of the PI controller will be investigated. Several parameters play a significant role: the input acceleration magnitude and frequency, the feedback gain and the gain of the controller. The first simulation carried out investigated the coding accuracy for the steady state in a system without a PI controller for feedback voltages, ' V_F ', applied to the plates of 20, 30 and 40 V; the input signal was a slow ramp in acceleration which changed from -1 to +1 g over a period of two seconds; this signal can be considered as a quasi-stationary signal. In the simulation two conventional second order Butterworth low-pass filters were used to attenuate the quantization noise in the digital bitstream. The two filters had cut-off frequencies which were not an integer multiple of each other as some coding pattern may introduce frequencies that are much lower than the limit cycle frequency and could distort the output signal. Fig. 7.13 shows the filter output signal; the nonlinearity in the first part of the curve is due to the transient time of the filter; around zero acceleration the simulation

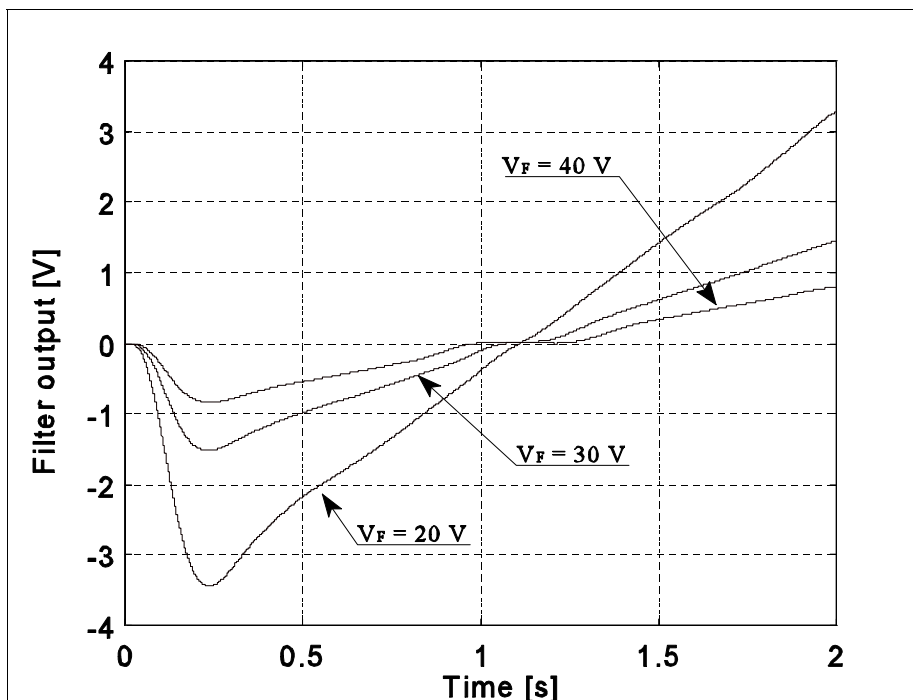


Fig. 7.13: Response of the digital accelerometer to a slow ramp in acceleration from -1 to +1 g. Obviously the lower the feedback voltage the more linear the transfer characteristic becomes.

illustrates the existence of a deadzone in the transfer characteristic, the width of which decreases with the feedback voltage. The deadzone can be explained by inspection of fig. 7.8 showing the movement of the seismic mass and the zero-order-hold and relay output in the unforced condition. The presence of a static acceleration will add a bias component to the movement of the seismic mass caused by the limit cycle. In order to cause the relay to change the output coding pattern, i.e. to code the input acceleration signal, the bias component magnitude has to be larger than the magnitude at the sampling point closest to the zero axis. In fig. 7.8 the second sample in a half-cycle is closest to the zero axis, with the seismic mass displaced by $0.19 \mu\text{m}$. This corresponds to a static acceleration of approximately $\pm 0.2 \text{ g}$ which agrees quite well with the simulation result shown in fig. 7.13 where the deadzone is approximately 0.35 s wide corresponding to an acceleration of $\pm 0.175 \text{ g}$. If the feedback voltage is decreased the deflection caused by an input acceleration becomes more significant since the deflection caused by the limit cycle decreases, hence the system starts to code at a lower input acceleration.

The drawback of decreasing the feedback voltage is a decrease of dynamic range of the

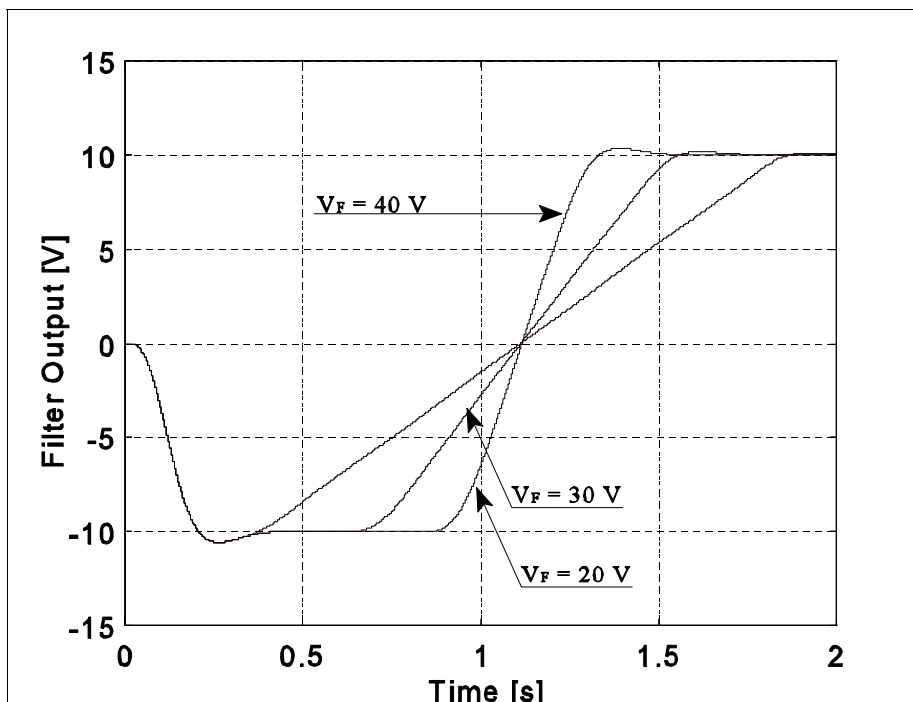


Fig. 7.14: Response of the accelerometer to a ramp in acceleration from -15 g to $+15 \text{ g}$. The higher the feedback voltage the higher the dynamic range of the device.

accelerometer. Fig. 7.14 shows the response of the system to a slow ramp in acceleration from -15 to +15 g in two seconds. It is obvious that the acceleration magnitude at which the system saturates decreases with the feedback voltage. With the above considerations it is clear that the choice of the feedback voltage enables a trade-off between the dynamic range and the coding accuracy and hence the resolution of the digital accelerometer.

The introduction of a PI controller which converts the system to type one can improve the coding accuracy. Fig. 7.15 shows the response of the system to the -1 to +1 g ramp in acceleration again over two seconds, using a feedback voltage of 40 V, unity proportional gain and an integral gain of 100. Compared with fig. 7.13 this resulted in a considerable improvement as the deadzone virtually disappeared. The limitation of the PI controller lies in the transient time the system requires until it starts to code accurately. The transfer characteristic of fig. 7.15 is not a perfect straight line due to the fact that the ramp is too fast for the system to code accurately.

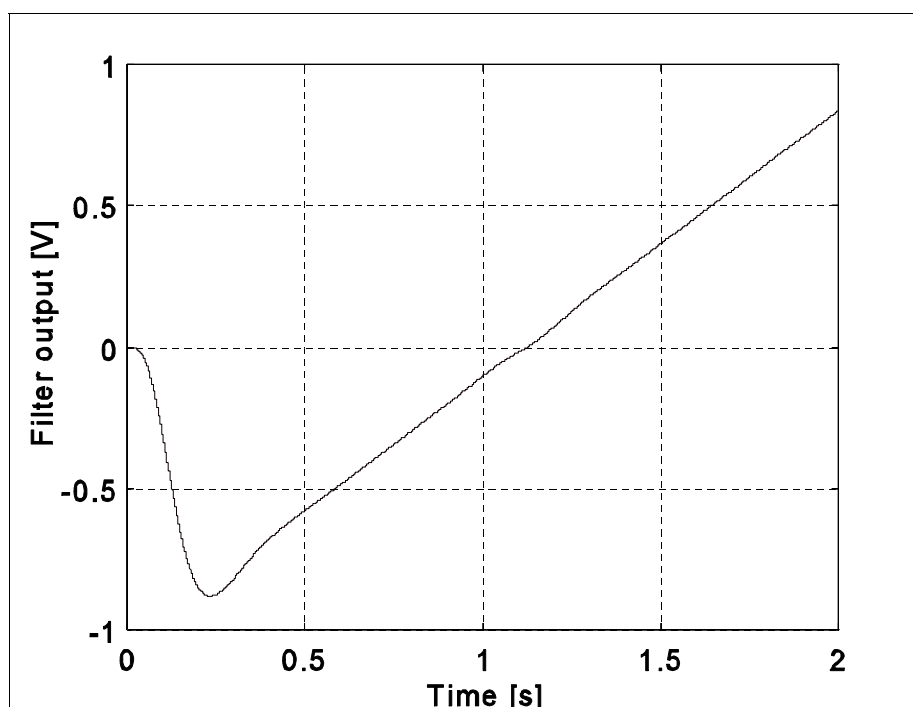


Fig. 7.15: Response of the system to a ramp in acceleration with a PI controller for $V_F = 40$ V. Compared to fig. 7.13 the deadzone has virtually disappeared.

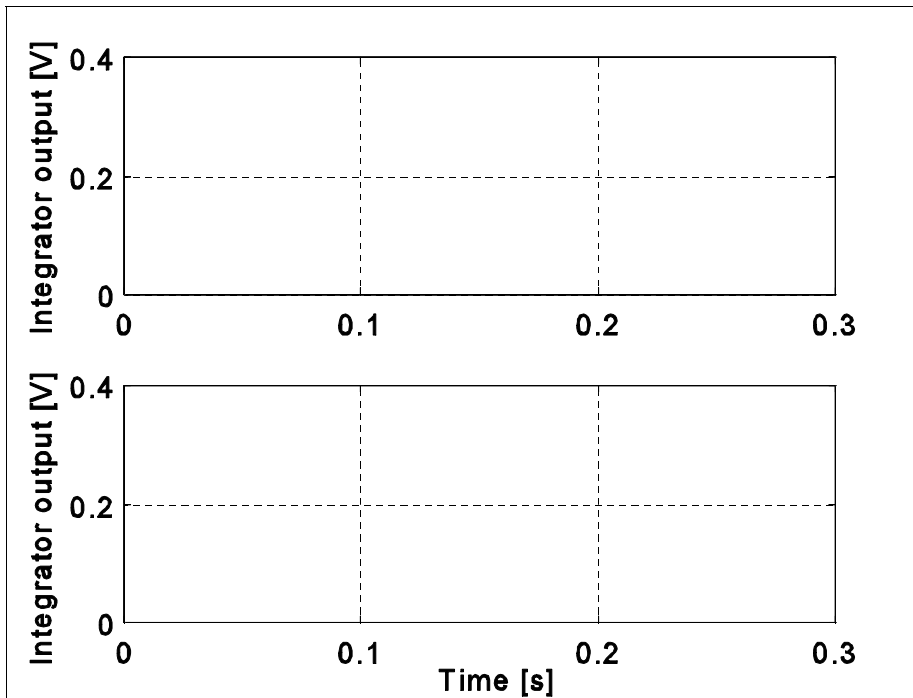


Fig. 7.16: Integrator output for 0.01 g (top trace) and 0.02 g (bottom trace) input acceleration. The transient time of the system is determined by the instant the integrator starts to ramp down the first time.

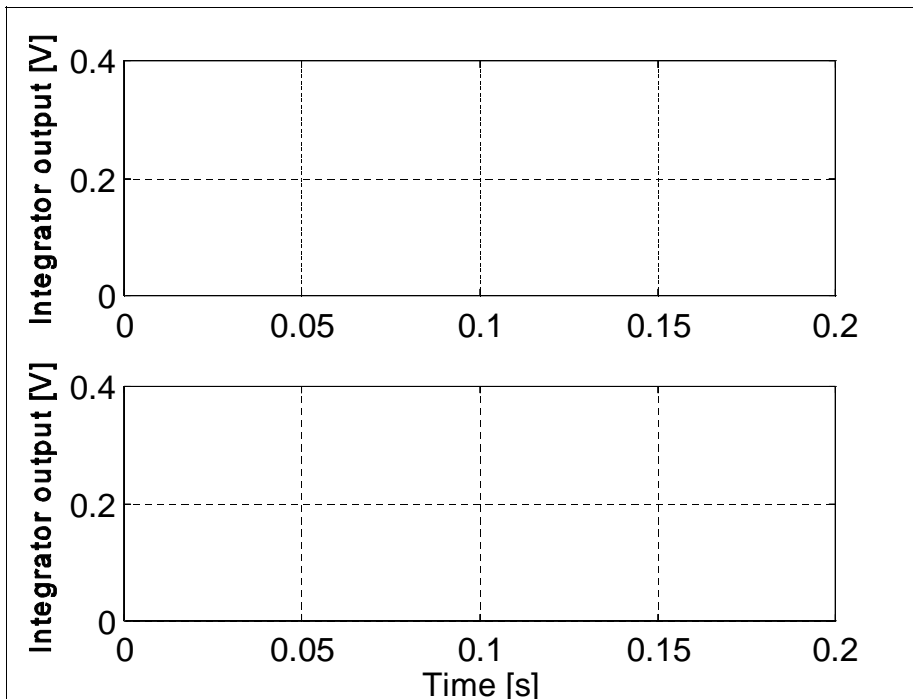


Fig. 7.17: Integrator output for the same parameters as in fig. 7.16, but the integrator gain was doubled. The transient time of the system was halved.

The transient time required for the digital accelerometer to code accurately is inversely proportional to the integral gain and proportional to the magnitude of the input acceleration. Fig. 7.16 illustrates this point in which a constant input acceleration of 0.01 g was assumed for the upper trace and 0.02 g for the lower trace. The traces show the output signal of the integrator. The integrator accumulates the constant input signal; the time at which accurate coding commences can be identified by determining the time period at which the integrator starts to ramp down the first time. For the upper trace this is approximately 0.19 s; for the lower 0.09 s. The bandwidth of this system can be determined for a given resolution, i.e. for a resolution of 0.01 g the bandwidth can be found as $1/0.19 \text{ s} = 5.3 \text{ Hz}$ and for 0.02 g resolution as 11.1 Hz. These values indicate a too low bandwidth; this can be improved by an increase in integral gain as shown in fig. 7.17 where the integral gain was doubled to 200. It is obvious that the transient time of the system was halved, hence the bandwidth doubled. Again it should be recalled here that these values cannot to be expected to be very accurate as the mathematical model simplifies the real device considerably.

Table 7.2 shows a summary of the above findings.

Results in: In-crease in:	Bandwidth	Resolution	Dynamic range
Sampling frequency	increase	increase	no effect
Feedback voltage	increase	decrease	increase
Integral gain	increase	increase	no effect

Table: 7.2: Effects of the main system parameters on the accelerometer performance.

7.3.4 Larger Deflections of the Seismic Mass

Similar to the analysis of the analogue, closed loop accelerometer the condition for which the

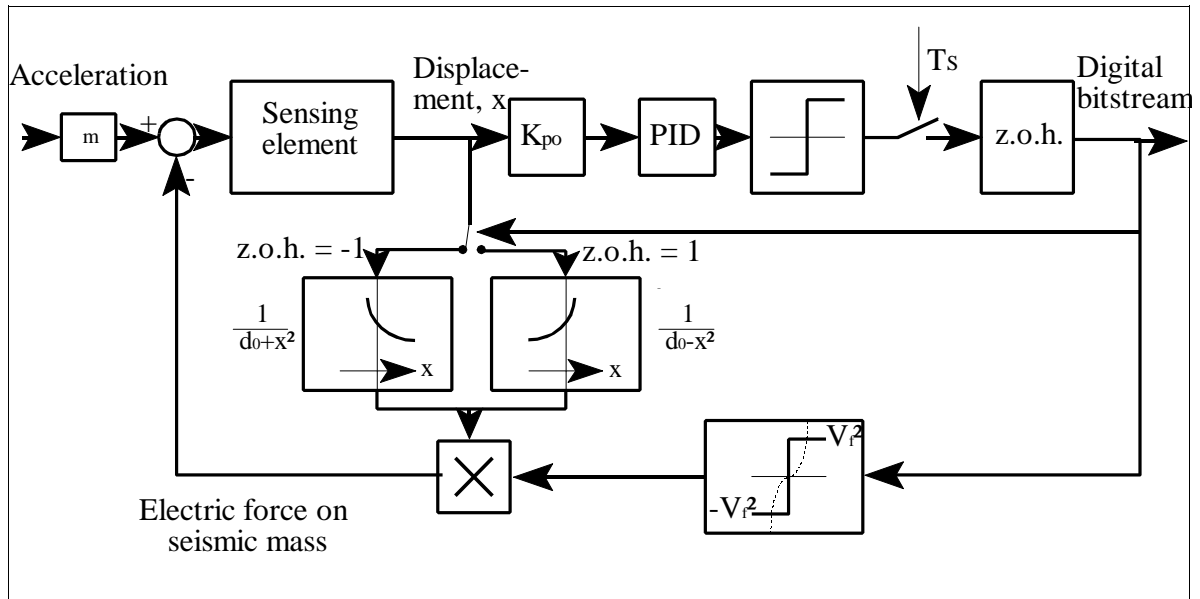


Fig. 7.18: Mathematical model of the digital accelerometer considering larger deflection of the seismic mass.

assumption of small deflections of the seismic mass is violated, will be investigated. The mathematical model of the digital accelerometer can be represented by the block diagram model shown in fig. 7.18 in which the influence of the position of the seismic mass on the electrostatic force and on the damping coefficient is considered. The electrostatic force is calculated by multiplying the square of the feedback voltage with the inverse square of the distance between the seismic mass and the electrode to which the feedback voltage is applied. Whether the top or bottom electrode has to be considered is determined by a switch controlled by the current state of the z.o.h.

Fig. 7.19 shows the implementation of the model in SIMULINK. The simulation result for the unforced condition is shown in fig. 7.20 where the top trace depicts the relay output and the bottom trace the movement of the seismic mass. In comparison to the simulation in which the influence of the seismic mass on the feedback force was neglected, the limit cycle mode changes from a (1,1) mode to (2,2) mode in periodic intervals after a transient time. A further difference is that the amplitude of the deflection of the seismic mass is $0.22 \mu\text{m}$ for the (2,2) mode which is approximately one third less than the calculated value. This can be explained by the fact that the further the seismic mass is away from the central position the smaller the

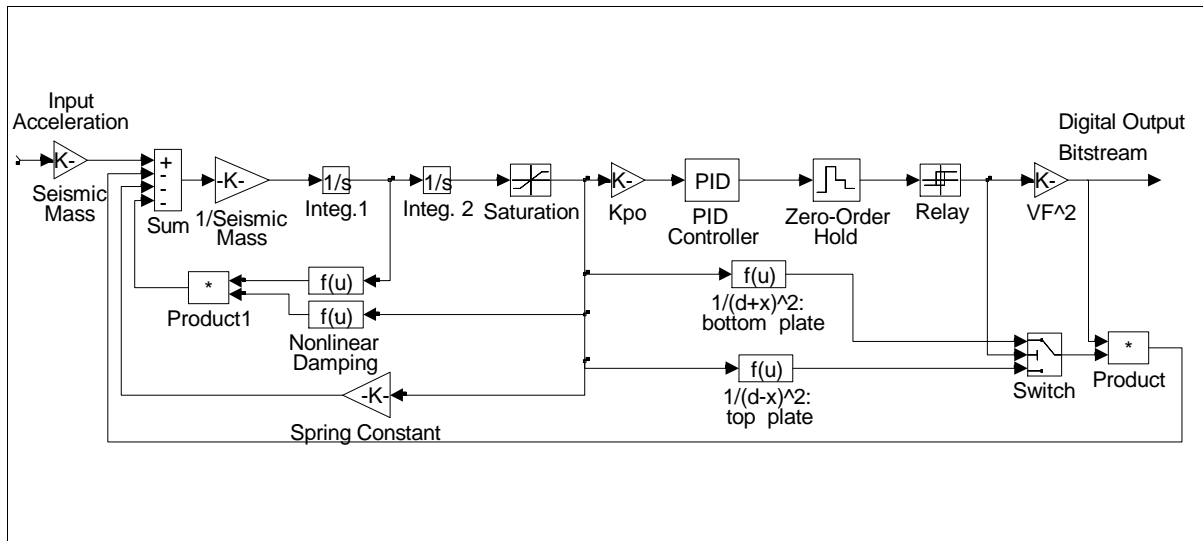


Fig. 7.19: SIMULINK model of the digital accelerometer incorporating the effect of the deflection of the seismic mass on the electrostatic force and the damping coefficient.

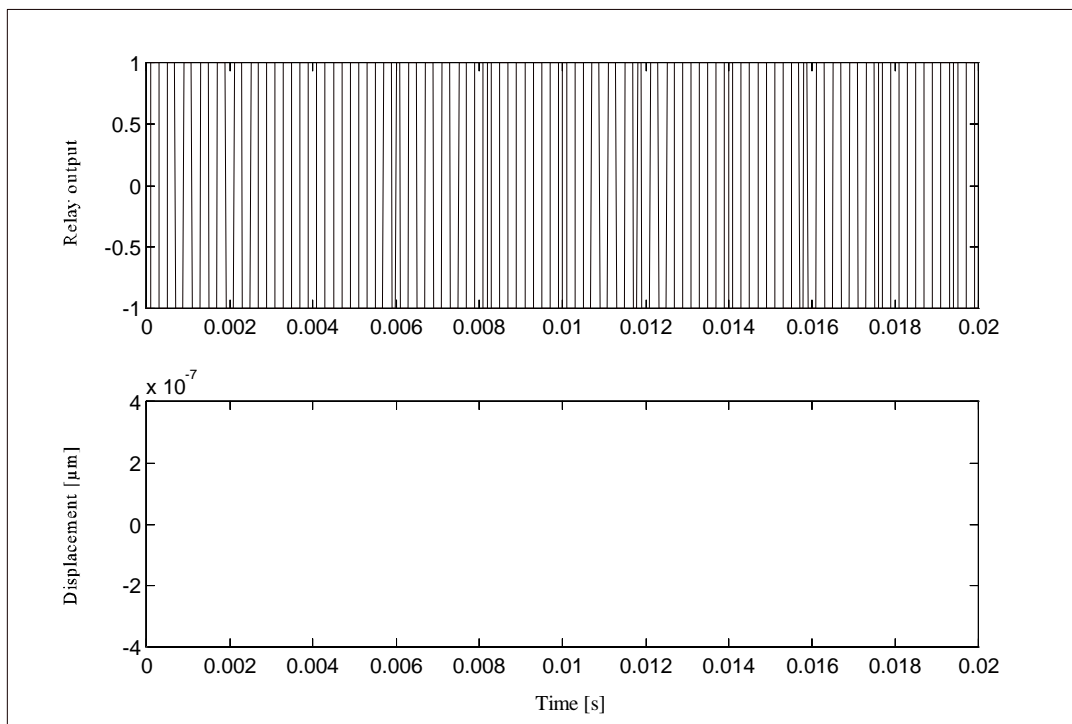


Fig. 7.20: Simulation result indicating that the limit cycle changes from a (1,1) mode to a (2,2) mode in regular intervals. Top trace: relay output; bottom trace: displacement of the seismic mass.

electrostatic force becomes; effectively the feedback gain is reduced. However, the bitstream is still a symmetrical waveform, hence no performance limitation is expected from the mode jumping.

A second simulation with a 50 Hz sinusoidal input acceleration was carried out; fig. 7.20 shows the bitstream (top trace), in this resolution it is just possible to identify the pulse density modulation. The middle trace shows the phase corrected output signal of the standard fourth order Butterworth filter with a corner frequency of 60 Hz to which the bitstream was subjected and the bottom trace is the input acceleration signal. The accuracy of the coding was determined by the simple expedient of comparing the sinusoidal input signal with the filtered output signal which is clearly sinusoidal.

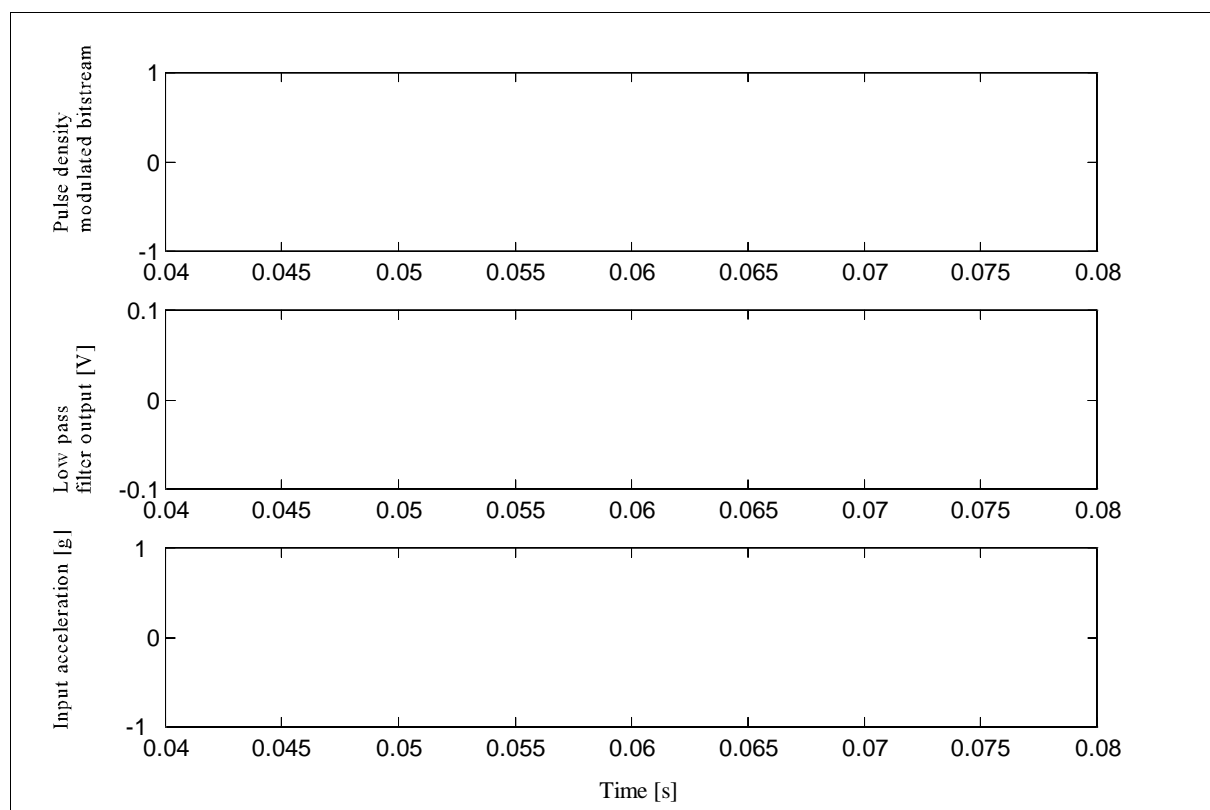


Fig. 7.20: Simulation result showing the response of the SIMULINK model to a 1 g, 50 Hz input acceleration. Top trace: pulse density modulated bitstream; bottom trace: output signal of the low pass filter.

The maximum deflection of the seismic mass in the above simulation was $\pm 0.3 \mu\text{m}$ consequently the maximum variation of the electrostatic force was about 6 % from the value with zero deflection.

A discrepancy between the simulation model and the real device became apparent while attempting to verify the improved system stability. If a shock in acceleration is assumed, which

led to a 'latch up' situation for the analogue accelerometer (see sec. 6.3), the digital accelerometer is expected to recover after the shock. However, due to the nature of the simulation model the integrators in the forward path accumulate a large signal even after the signal representing the position of the seismic mass is in saturation. Consequently, the physical meaning of the output of the first integrator, the velocity of the seismic mass, is not valid anymore, since the velocity of the mass is zero if the mass touches the electrodes; in a simulation this is not the case. Due to this discrepancy the recovery time after a shock is much longer than expected in reality, consequently no simulation results are presented here.